User Guide

SIB332
32 Channel APD Array Interface Board
Hamamatsu S8550 series

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

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General Safety Precautions

Use Proper Power Source

The SIB332 is powered with a +5V power source directly from Vertilon's PhotoniQ multi-channel data acquisition systems. Use with any other power source may result in damage to the product.

Operate Inputs within Specified Range

To avoid electric shock, fire hazard, or damage to the product, do not apply a voltage to any input outside of its specified range.

Electrostatic Discharge Sensitive

Electrostatic discharges may result in damage to the SIB332. For these reasons, the SIB332 board is intended to be operated in a user's conductive instrument enclosure.

Do Not Operate in Wet or Damp Conditions

To avoid electric shock or damage to the product, do not operate in wet or damp conditions.

Do Not Operate in Explosive Atmosphere

To avoid injury or fire hazard, do not operate in an explosive atmosphere.

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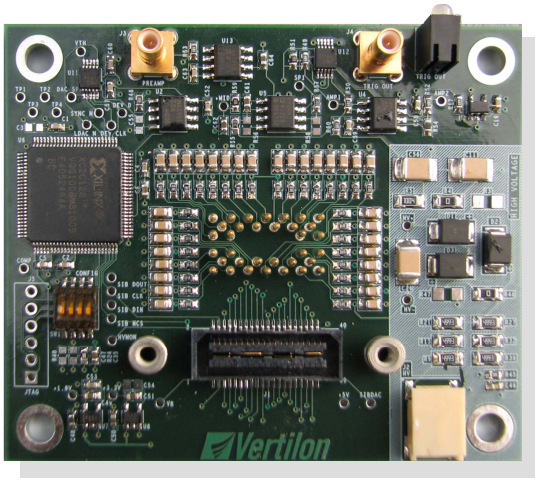
Product Overview

- Mounting board for Hamamatsu S8550 4 x 8 channel APD Array
- Provides 32 channel interface to Vertilon PhotoniQ DAQ systems
- Separate high voltage input for APD array bias
- High speed preamplifier for cathode current monitoring
- Leading edge discriminator for event trigger and timing
- 100% compatible with Vertilon's PhotoniQ multichannel DAQs
- Simplified control through PhotoniQ graphical user interface
- No external power supply required



The SIB332 APD array interface board provides the mechanical and electrical connectivity between the Hamamatsu S8550 4 x 8 element APD array and external signal processing electronics such as Vertilon's PhotoniQ multichannel data acquisition systems. The S8550 is mounted to the bottom side of the SIB332 through 34 socket pins that connect the APD array's 32 anode signals and two common cathodes to the board. The anode signals are routed through AC coupling capacitors to a connector located on the top of the board that connects to a specialized high density coaxial cable assembly. This arrangement allows the SIB332 to be conveniently mounted directly into the user's optical setup with the APD array facing outward from the bottom of the PCB and the sensor interface board (SIB) cable exiting from the top. The SIB cable carries the 32 anodes from the S8550 to the PhotoniQ where the charge from each is separately integrated, digitized, and sent to a PC for display or further signal processing. The negative high voltage bias to the APD array is supplied directly from the PhotoniQ on a high voltage cable to a dedicated connector on the SIB332. For applications requiring event timing from the S8550, the SIB332 includes a high speed preamplifier and a leading edge discriminator whose outputs are available on SMB connectors. The discriminator's threshold is fully adjustable using the PhotoniQ graphical user interface.

The various functions on the SIB332 are described in greater detail on the following pages. When necessary, refer to the functional block diagram shown in Figure 1 below.

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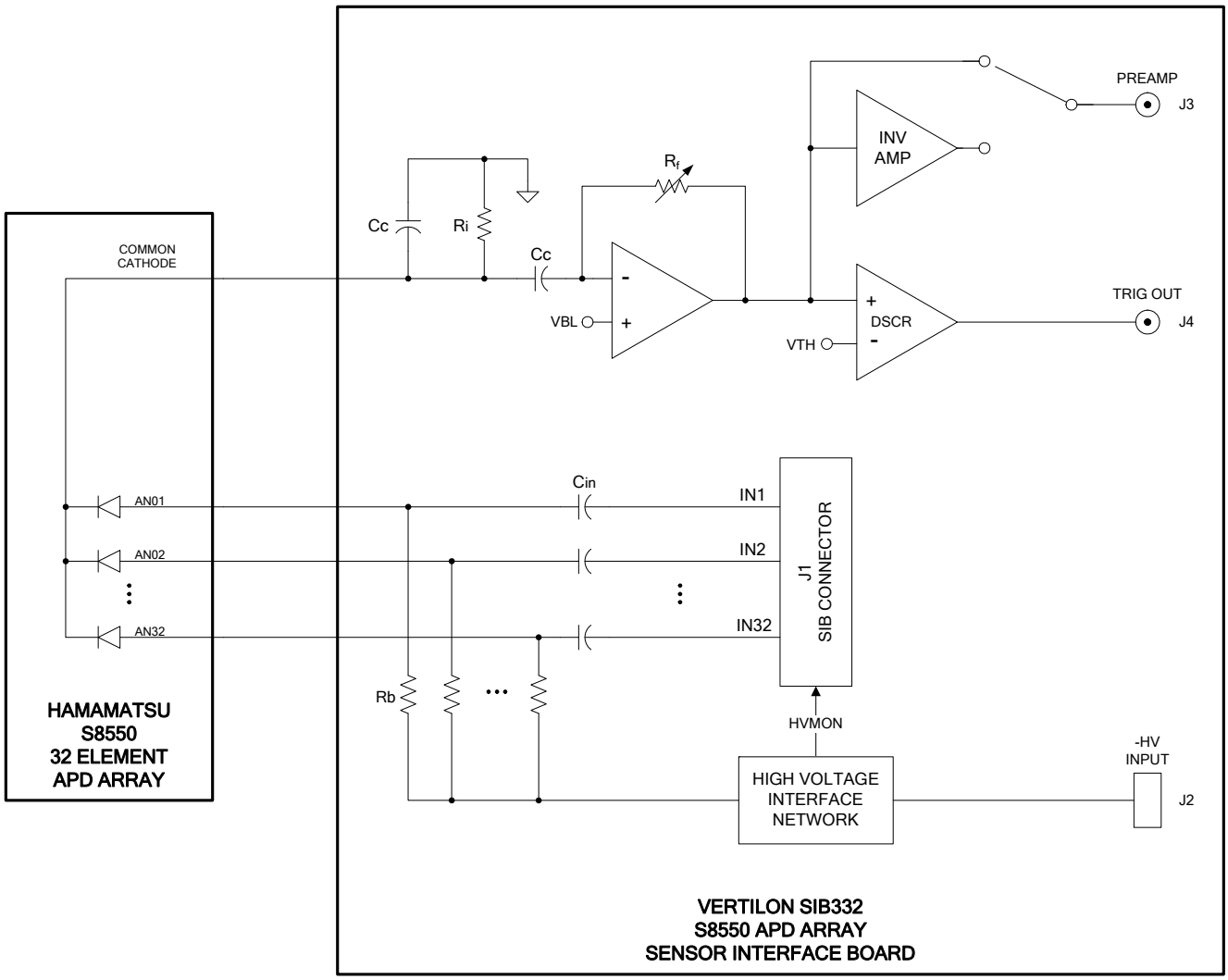

Figure 1: Functional Block Diagram

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Specifications

(T_A = +25C, unless otherwise noted)

Description	Sym	Min	Typ	Max	Units	Notes
HIGH VOLTAGE						
Array Bias Divider Ratio			0.5			Actual bias to array is ½ of voltage applied at connector J2.
High Voltage Input Load Resistance			3		MΩ	Measured at high voltage input connector, J2
High Voltage Input to HVMON Ratio			150			±10%
ANODE CIRCUITS						
Quantity	AN1 - AN32		32			
Bias Resistance	R_b		1		MΩ	
Preamplifier Coupling Capacitance	C_{in}		0.01		uF	
CATHODE CURRENT PREAMPLIFIER						
Input Coupling Capacitance	C_c		1000		pF	
Transimpedance (Low Gain)	R_f		150		Ω	
Transimpedance (High Gain)	R_f		550		Ω	
Inverting Stage Gain			2		V/V	
Preamp Baseline Level	V_{BL}		+0.50		V	
Preamp Output Impedance			50		Ω	Measured at preamplifier output, J3
LEADING EDGE DISCRIMINATOR						
Threshold Adjustment Range	V_{th}	+0.50		+2.50	V	Referenced to baseline level at discriminator input. Threshold (0 to 100%) controlled through GUI interface.
Threshold to Output Delay	t_d		7		nsec	
TRIGGER OUTPUT						
Output Impedance			50		Ω	
Logic High Output Level	V_{OH}	+4.3	+4.8		V	(I_{OH} = -32mA)
Logic Low Output Level	V_{OL}		+0.2	+0.6	V	(I_{OL} = 32mA)
DIMENSIONS						
Width	W		76		mm	
Length	L		64		mm	
Thickness	T		1.57		mm	(printed circuit board only)

Table 1: Specifications

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Typical Setup

In a typical setup the Hamamatsu S8550 array is plugged into the SIB332 Sensor Interface Board (SIB) which in turn connects to a Vertilon PhotoniQ IQSP480 or IQSP580 multi-channel data acquisition system using a SIB cable. Negative bias to the APD array is supplied and controlled by the PhotoniQ through a specialized high voltage cable. When triggered from the trigger output on the board or from an external source, the PhotoniQ integrates and digitizes the 32 charge signals from the array and outputs a data packet to the PC over a USB connection.

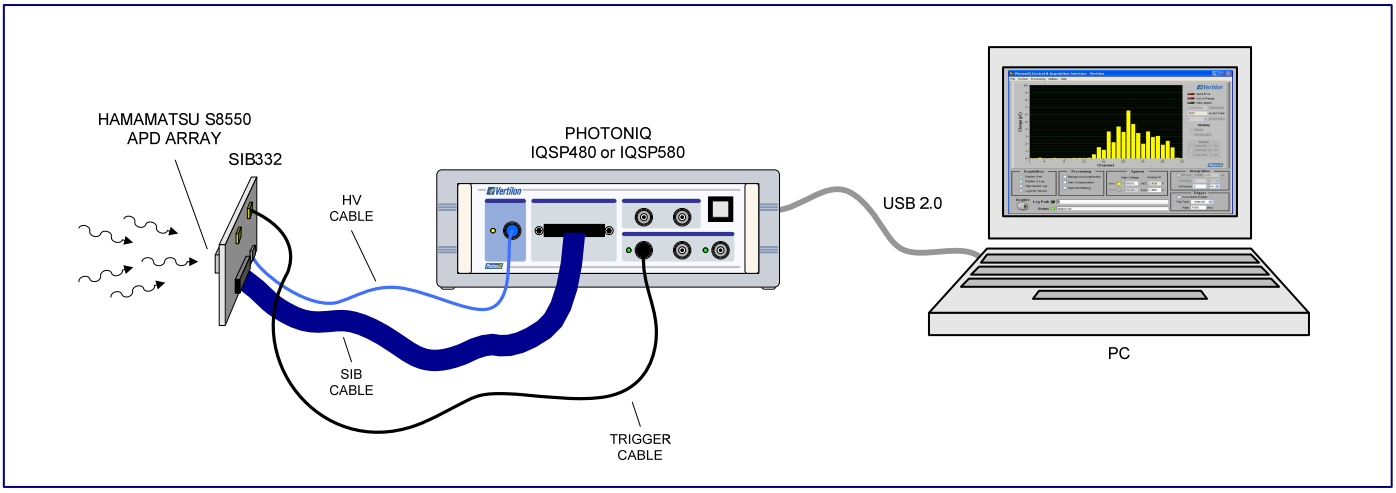

Figure 2: Typical Setup

High Voltage Interface

The SIB332 employs the interface circuit shown below between the high voltage input connector, J2, and the internal high voltage bias to the S8550. Because the interface circuit utilizes a two to one voltage divider, the actual bias voltage applied to the APD array is half of the voltage supplied on connector J2. The monitor output (HVMON) allows the high voltage bias for the APD array to be indirectly monitored at a reduced voltage level. Voltage readings at the monitor point should be scaled by a factor of 150. Calibration of the scale factor may be required.

> Warning: The high voltage section of the SIB332 contains signals at voltage levels that can exceed negative 1500 volts. Never touch a component or signal in this area.

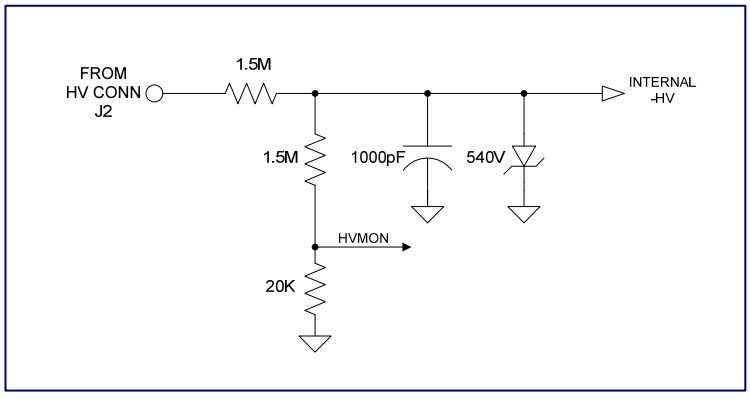

Figure 3: APD Array High Voltage Interface Circuit

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APD Array Anode Circuits

The 32 anode signals (AN1 – AN32) from the S8550 APD array are AC-coupled through capacitors on the SIB332 to a specialized connector (J1) referred to as the sensor interface board (SIB) connector. The SIB connector mates to a proprietary low-noise, high density SIB cable assembly that carries the 32 anode signals on coaxial connections to a Vertilon PhotoniQ 32 channel charge integrating data acquisition system. Depending on the required speed and dynamic range, either a PhotoniQ IQSP480 high dynamic range system or an IQSP580 high speed system can be used as the main data acquisition unit. Figure 4 below illustrates the equivalent circuit as seen by each APD array anode. Each detector anode is coupled to its respective transimpedance amplifier in the PhotoniQ through a 0.01uF capacitor. With the common cathode of the array effectively grounded, the negative high voltage bias to each detector is applied through individual 1.0 Mohm resistors. Note, because the Hamamatsu S8550 APD array is of the common cathode type, the current polarity to the PhotoniQ preamplifiers is *into* its inputs. For this reason, the *Input Polarity* under the *Data Configuration* menu in the PhotoniQ GUI should be set to *negative*. See the PhotoniQ user's manual for more details.

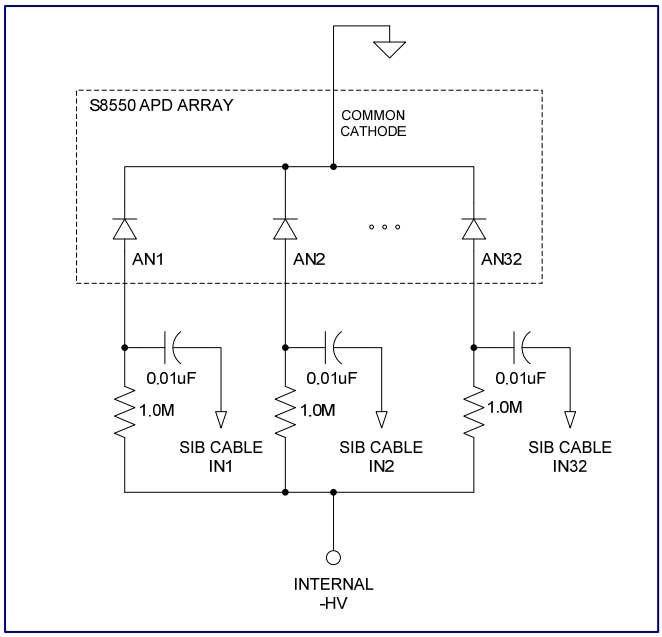

Figure 4: APD Array Anode Circuits

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Cathode Current Preamplifier

This preamplifier is designed for small negative current pulses from the common cathode of the S8550 APD array. Through the dialog box shown below, the user can set its gain to either *low* or *high* and the polarity of its output that is available on SMB connector, J3. The preamplifier signal is further processed on the SIB332 by the leading edge discriminator to generate trigger signals in sync with the current pulse on common cathode. Alternatively, for applications requiring external discrimination of the cathode signal, the preamplifier output can be directly connected to other equipment.

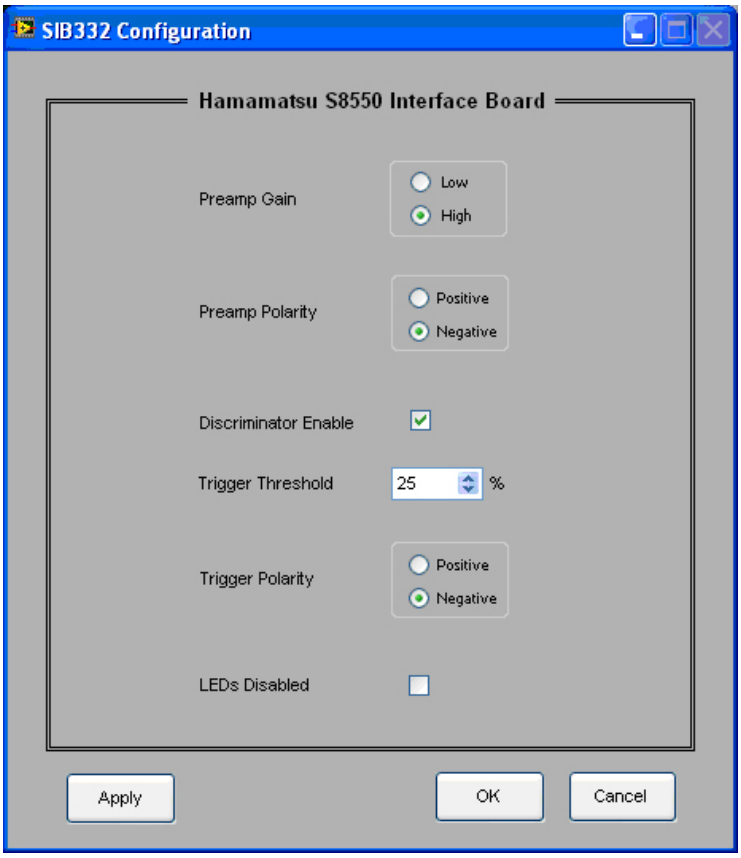

Figure 5: SIB332 Dialog Box

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Leading Edge Discriminator

The leading edge discriminator generates a logic signal when a pulse from the preamplifier exceeds a user-defined threshold. The SIB332 GUI dialog box allows the user to set this threshold between 0 and 100% where 100% is equal to the maximum possible signal amplitude in the discriminator channel. When a pulse is detected, the trigger output from the board becomes active. The polarity can be set to either *positive* or *negative*.

Figure 6 shows the operation of the leading edge discriminator. A negative-going current pulse into the preamplifier results in a positive-going pulse on its output. This pulse is compared to a threshold that is adjusted using the SIB332 dialog box in the PhotoniQ GUI. A logic high (for *positive* polarity control) is generated after a small delay (t_d) from when the pulse first crosses the threshold, V_{th}. The discriminator switches back to a logic low when the pulse crosses the threshold from the opposite direction as it returns back to the baseline level. The trigger LED blinks when a trigger signal is generated.

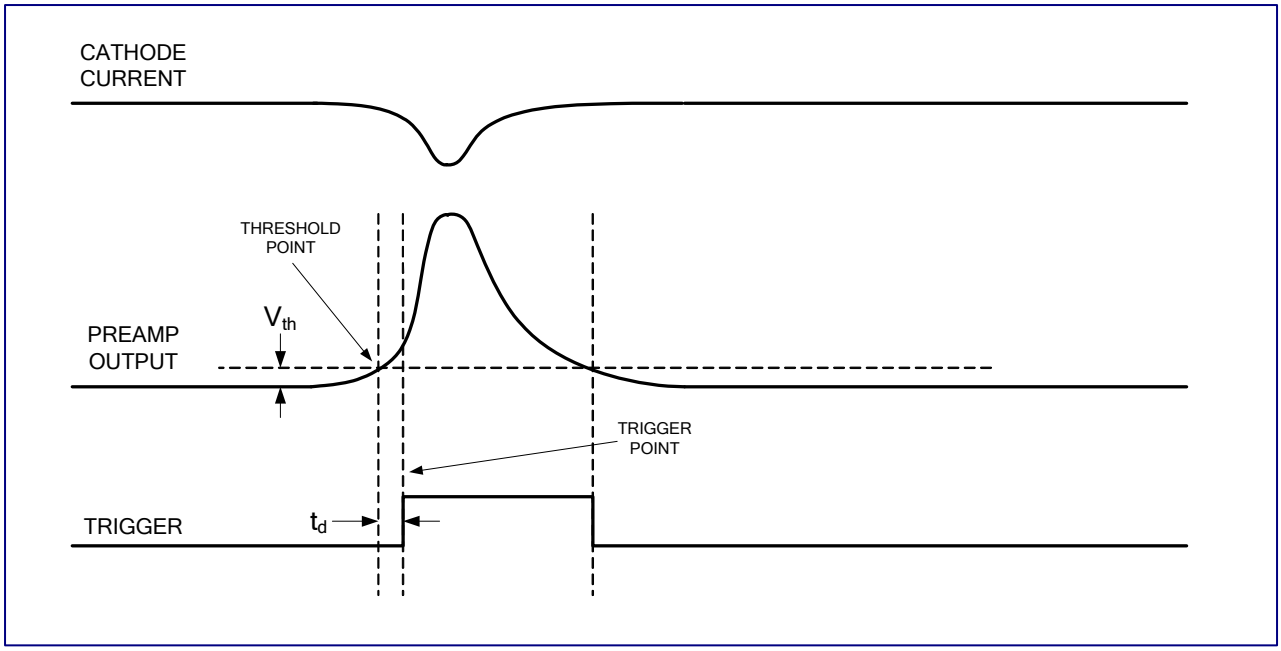

Figure 6: Leading Edge Discriminator Timing

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Top and Bottom Views

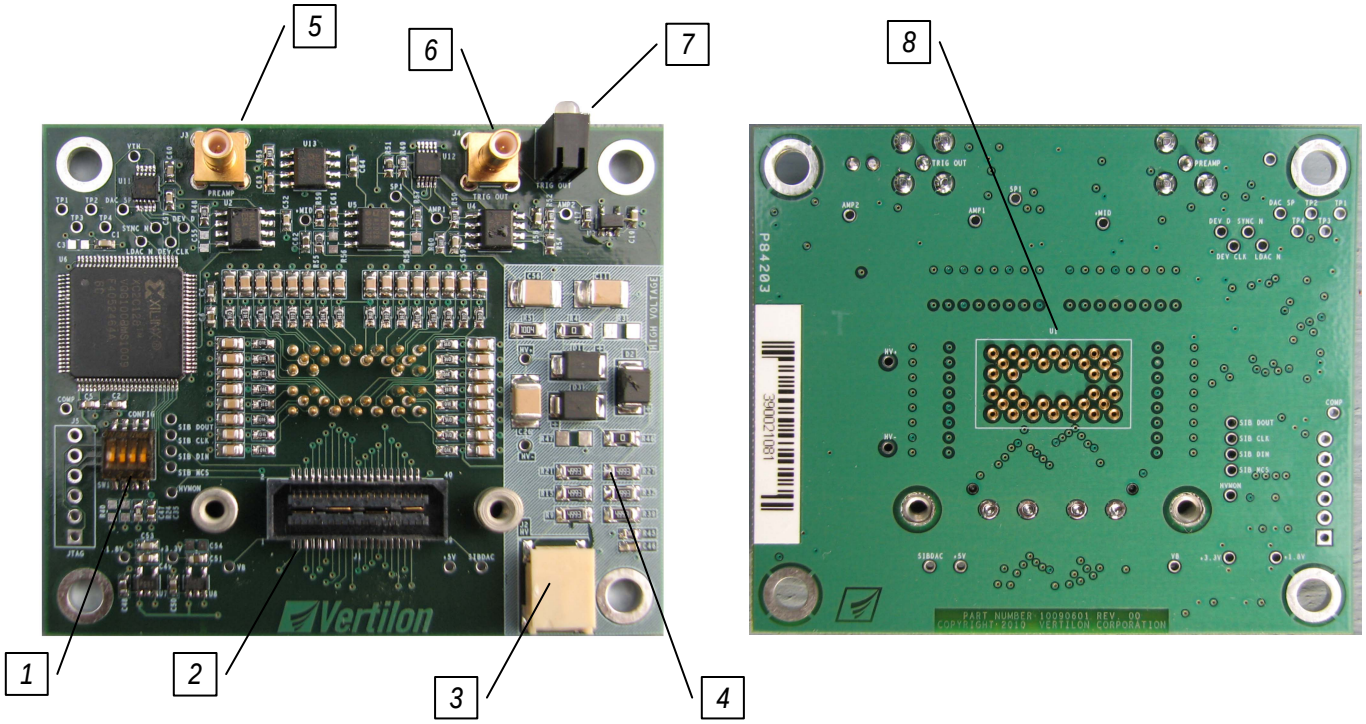

Figure 7: Top and Bottom Views

1. Configuration Switches (SW1)
2. Sensor Interface Board Connector (J1)
3. High Voltage Input (J2)
4. High Voltage Section
5. Preamp Output (J3)
6. Trigger Output (J4)
7. Trigger LED
8. S8550 Socket Pins

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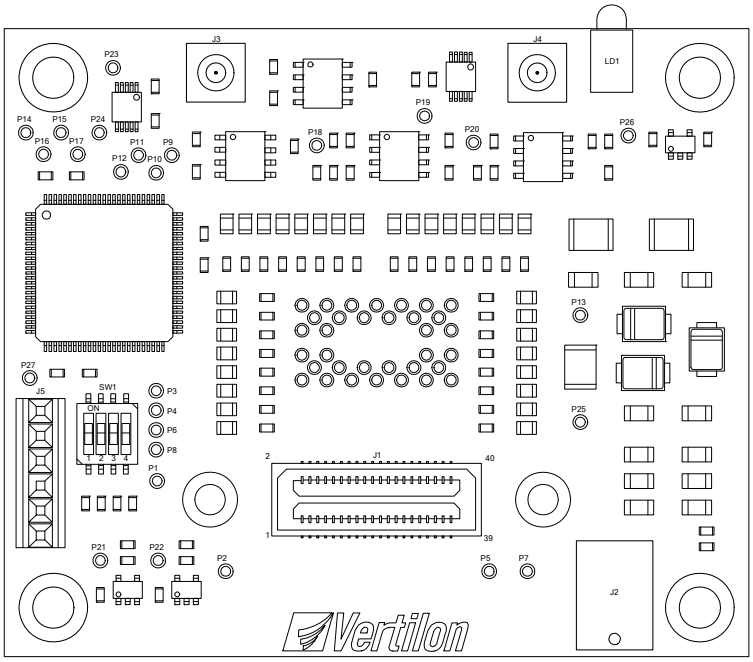

Figure 8: Component Locations and Functions

Name	Function	Description
J1	CHANNELS 1 - 32	Sensor interface board connector to SIB cable for channels 1 -32
J2	-HV	Negative high voltage bias input
J3	PREAMP	Cathode current preamplifier output
J4	TRIG OUT	Leading edge discriminator output
J5	JTAG	JTAG interface
LD1	TRIG OUT	LED indicator for trigger output
SW1: 1-2	DEV ADDR 1:0	Sets the device address for control by the PhotoniQ. Set both switches to “ON”.
SW1: 3-4	DEV TYPE 1:0	Sets the device type for control by the PhotoniQ. Set both switches to “ON”.

Table 2: Connectors, LEDs, and Switches

Name	Ref #	Description
+5V	P5	Main +5V power to the SIB332 supplied by the PhotoniQ through SIB connector J1.
+MID	P18	Baseline voltage for cathode current signal processing chain. Nominally +0.5V.
-HV	P25	APD array bias. Warning: This is a high voltage point that can exceed negative 1500 volts.
HVMON	P1	Attenuated version of –HV used for indirectly monitoring APD array bias.
AMP1	P20	Output of cathode current preamplifier.
AMP2	P26	Output of cathode current second stage inverting amplifier.
VTH	P23	Threshold voltage to leading edge discriminator.

Table 3: Test Points

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S8550 to PhotoniQ Mapping

The table below shows the mapping of the S8550 anodes to the PhotoniQ input channels.

S8550 Signal	PhotoniQ Channel	S8550 Signal	PhotoniQ Channel	S8550 Signal	PhotoniQ Channel	S8550 Signal	PhotoniQ Channel
A1	1	A2	9	A3	17	A4	25
B1	2	B2	10	B3	18	B4	26
C1	3	C2	11	C3	19	C4	27
D1	4	D2	12	D3	20	D4	28
E1	5	E2	13	E3	21	E4	29
F1	6	F2	14	F3	22	F4	30
G1	7	G2	15	G3	23	G4	31
H1	8	H2	16	H3	24	H4	32

Table 4: S8550 to PhotoniQ Mapping

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SIB Connector Pinout

The SIB332 connectors and cables are fully compatible with all Vertilon PhotoniQ systems. For applications utilizing data acquisition systems other than Vertilon's PhotoniQ series, the pinout for connector J1 is provided in Table 5 as a reference.

J1			
Signal Name	Pin #	Signal Name	Pin #
VB	1	HVMON	2
SIB_DIN	3	SIB_CLK	4
P16	5	P32	6
P15	7	P31	8
P14	9	P30	10
P13	11	P29	12
P12	13	P28	14
P11	15	P27	16
P10	17	P26	18
P9	19	P25	20
P8	21	P24	22
P7	23	P23	24
P6	25	P22	26
P5	27	P21	28
P4	29	P20	30
P3	31	P19	32
P2	33	P18	34
P1	35	P17	36
SIB_DOUT	37	SIB_NCS	38
SIBDAC	39	+5V	40

Table 5: Sensor Interface Board (SIB) Connector Pinout

Power (+5V) supplied through pin 40 if PhotoniQ is not used
Pins 3, 4, 37, 38, 39 used by PhotoniQ and should be left unconnected
Ground supplied through SIB cable shielding

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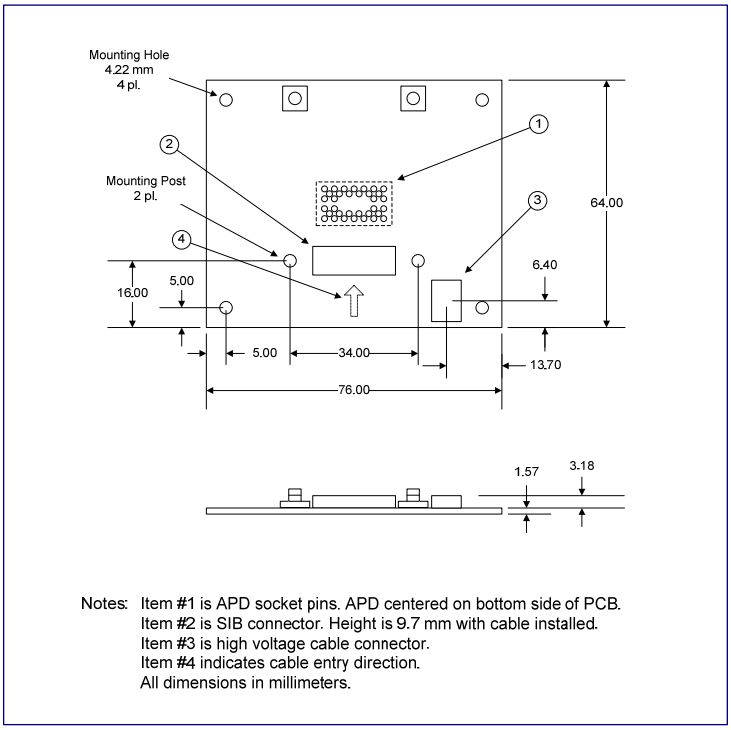
Mechanical Information



Notes: Item #1 is APD socket pins. APD centered on bottom side of PCB.
Item #2 is SIB connector. Height is 9.7 mm with cable installed.
Item #3 is high voltage cable connector.
Item #4 indicates cable entry direction.
All dimensions in millimeters.

Figure 9: SIB332 Printed Circuit Board Dimensions

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