User Guide

SIB164-1018
64 Channel MAPMT Interface Board
Hamamatsu H7546 series

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Disclaimer

Vertilon Corporation has made every attempt to ensure that the information in this document is accurate and complete. Vertilon assumes no liability for errors or for any incidental, consequential, indirect, or special damages including, without limitation, loss of use, loss or alteration of data, delays, lost profits or savings, arising from the use of this document or the product which it accompanies.

Vertilon reserves the right to change this product without prior notice. No responsibility is assumed by Vertilon for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under the patent and proprietary information rights of Vertilon Corporation.

Copyright Information

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Table of Contents

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

List of Figures

List of Tables

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

General Safety Precautions

Use Proper Power Source

The SIB164-1018 is powered with a +5V power source directly from Vertilon's PhotoniQ multi-channel data acquisition systems. Use with any other power source may result in damage to the product.

Operate Inputs within Specified Range

To avoid electric shock, fire hazard, or damage to the product, do not apply a voltage to any input outside of its specified range.

Electrostatic Discharge Sensitive

Electrostatic discharges may result in damage to the SIB164-1018. For this reason, the SIB164-1018 board is intended to be operated in a user's conductive instrument enclosure.

Do Not Operate in Wet or Damp Conditions

To avoid electric shock or damage to the product, do not operate in wet or damp conditions.

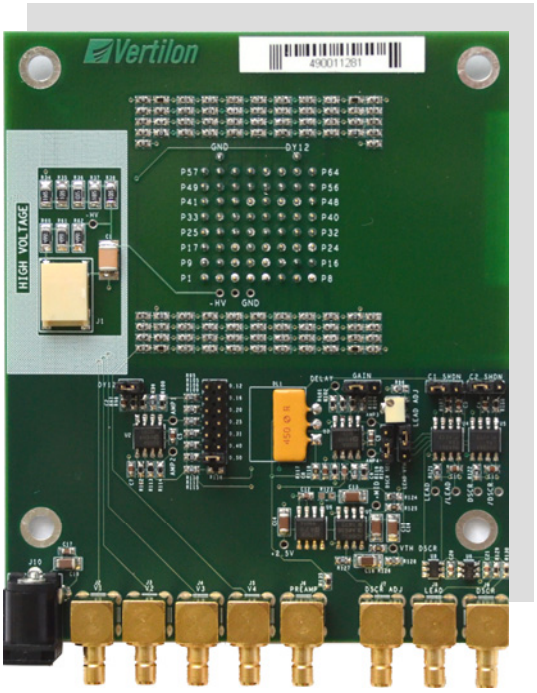
Do Not Operate in Explosive Atmosphere

To avoid injury or fire hazard, do not operate in an explosive atmosphere.

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Product Overview

- Mounting board for Hamamatsu H7546 64 channel MAPMT
- Includes anger logic for interface to data acquisition systems
- High speed preamplifier for last dynode output
- Leading edge, constant fraction, and zero slope discriminators
- Adjustable gain and discriminator thresholds
- Separate high voltage input for MAPMT cathode bias
- 100% compatible with Vertilon's PhotoniQ multichannel DAQs



The SIB164-1018 multianode photomultiplier tube interface board provides the mechanical and electrical connectivity between the Hamamatsu H7546 64 anode PMT and external signal processing electronics such as Vertilon's PhotoniQ multichannel data acquisition systems. The H7546 is mounted to the bottom side of the SIB164-1018 through 66 socket pins that connect the PMT's 64 anode signals, last dynode output, and high voltage input to the board. The anode signals are routed to an on-board resistive anger logic circuit that generates four anger signal outputs. These outputs connect using four coaxial cables to Vertilon's PhotoniQ IQSP418 or IQSP518 multichannel data acquisition system where the charge from each is separately integrated, digitized, and sent to a PC for display or further signal processing. For applications utilizing the last dynode output of the H7546, the SIB164-1018 includes a two stage high speed preamplifier whose output is available on an SMB connector. One of three on-board discriminators can be used with the last dynode signal to generate a trigger to the data acquisition system or other external electronics. The outputs from a leading edge, constant fraction, and zero slope discriminator — which respectively generate trigger signals based on threshold, percentage of pulse height, and pulse peak — are available on SMB connectors. Several user adjustments are included for optimizing system gain and trigger thresholds for the discriminators. When using an H7546A PMT, the negative high voltage bias to the PMT's cathode is supplied through its high voltage cable. This cable is compatible with the high voltage SHV output from the PhotoniQ. Alternatively, when using an H7546B, three optional socket pins can be added to the board for direct connection of the PMTs high voltage input. In this case, the high voltage bias is supplied through the SIB164-1018 on a specialized cable from the PhotoniQ.

The various functions on the SIB164-1018 are described in greater detail on the following pages. When necessary, refer to the functional block diagram shown in Figure 1 below.

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

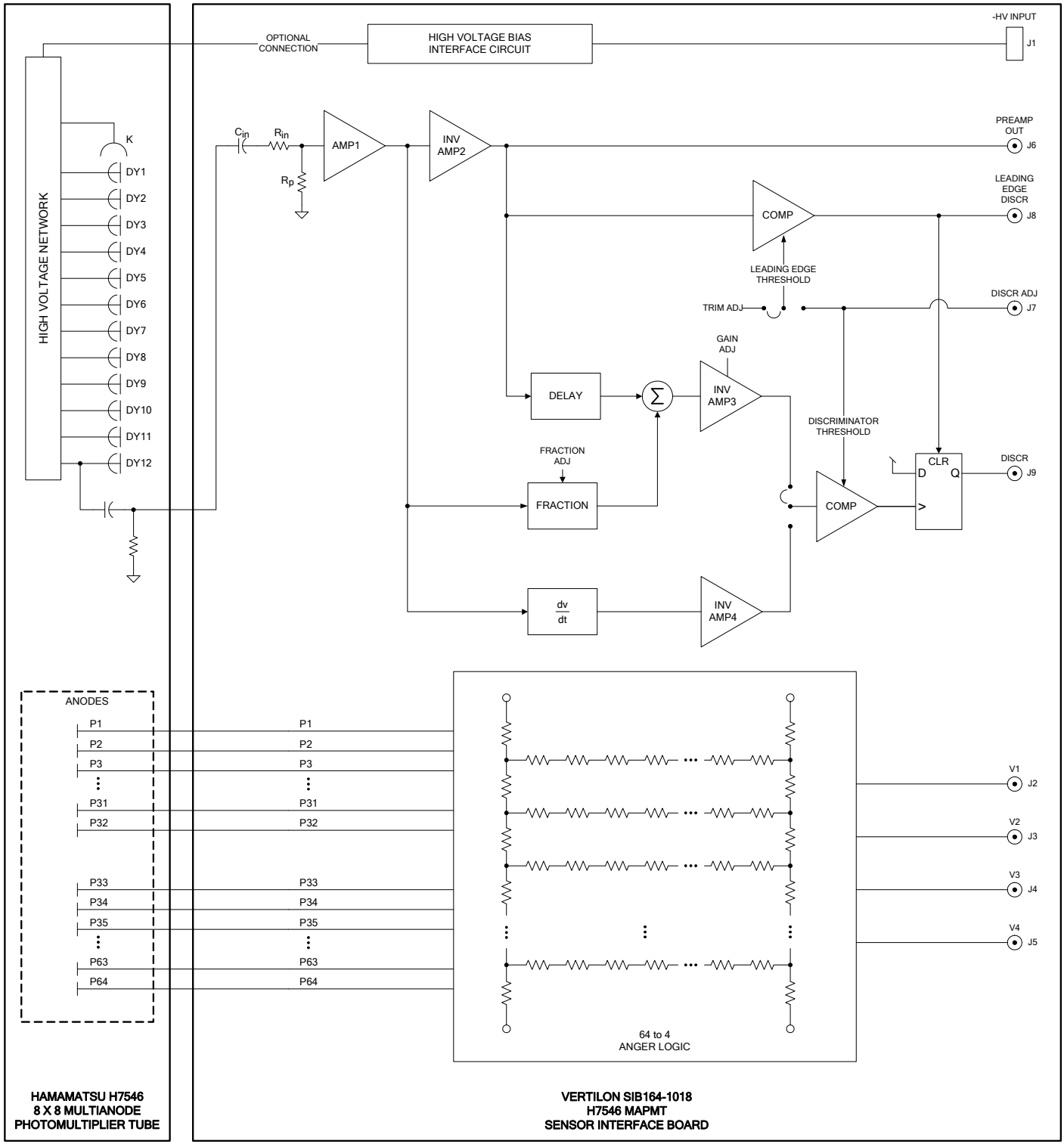


Figure 1: Functional Block Diagram

Specifications

(V_{supply} = +5.0V, T_A = +25C, unless otherwise noted)

Description	Sym	Min	Typ	Max	Units	Notes
HIGH VOLTAGE						
High Voltage Input Load Resistance			50		MΩ	Measured at high voltage input connector, J1
ANODE CIRCUITS						
Quantity	P1 - P64		64			
Input Bias Voltage			+0.250		V	Detector bias voltage supplied from PhotoniQ data acquisition system
LAST DYNODE PREAMPLIFIER						
Input Coupling Capacitance	C_{in}		0.1		uF	
Input Resistance	R_{in}		50		Ω	
Input Parallel Resistance	R_p		500		Ω	
Amplifier #1 Gain	A1		14.0		dB	
Amplifier #2 Inverting Gain	A2		6		dB	V_{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to preamplifier input at DY12.
Amplifier #2 Output Impedance			50		Ω	Measured at preamplifier output, J6
LEADING EDGE DISCRIMINATOR						
Threshold Adjustment (External)	V_{th1}	-100		0	mV	Referenced to baseline level at comparator input. Controlled using DSCR ADJ on J7 (+2.5V to +3.0V).
Threshold Adjustment (Internal)	V_{th1}	-50		0	mV	Referenced to baseline level at comparator input. Controlled using potentiometer VR1.
Threshold to Output Delay (V_{in}=30mV)	t_{d1}		5		nsec	
Time Walk (V_{in}: 3mV to 30mV)			-13		nsec	Output on connector, J8.
Time Walk (V_{in}: 30mV to 150mV)			-3.0		nsec	V_{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to preamplifier input at DY12. Threshold (V_{th1}) set to 15mV below the baseline.
Jitter (V_{in}: 10mV)				1	nsec	
CONSTANT FRACTION DISCRIMINATOR						
Delay	D		5		nsec	Standard delay element, other delays available.
Delay to Fraction Ratio		0.12		0.50		7 steps of 2 dB each Steps: 0.12, 0.16, 0.20, 0.25, 0.31, 0.40, 0.50
Amplifier #3 Inverting Gain	A3		+8.6		dB	Jumper JP3 in "left" position.
Threshold Adjustment	V_{th2}	0		+100	mV	Referenced to baseline level at comparator input. Controlled using DSCR ADJ on J7 (+2.5V to +2.0V).
Threshold to Output Delay (V_{in}=30mV)	t_{d2}		5		nsec	
Time Walk (V_{in}: 20mV to 100mV)			-1.5		nsec	Output on connector, J9.
Jitter (V_{in}: 50mV)				500	psec	V_{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to preamplifier input at DY12. Threshold (V_{th2}) set to 15mV above the baseline. Fraction set to 0.50.

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Description	Sym	Min	Typ	Max	Units	Notes
ZERO SLOPE DISCRIMINATOR						
Differentiator First-Order Time Constant			3.3		nsec	
Amplifier #4 Inverting Gain	A4		10.4		dB	
Threshold Adjustment	V_{th3}	0		+100	mV	Referenced to baseline level at comparator input. Controlled using DSCR ADJ on J7 (+2.5V to +2.0V).
Threshold to Output Delay (V_{in}=30mV)	t_{d3}		7		nsec	Output on connector, J9. V_{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to preamplifier input at DY12. Threshold (V_{th3}) set to 5mV above the baseline.
Time Walk (V_{in}: 20mV to 150mV)			-3.0		nsec	
Jitter (V_{in}: 100mV)				500	psec	
DISCRIMINATOR OUTPUTS						
Output Impedance			50		Ω	
Logic High Output Level	V_{OH}	+4.3	+4.8		V	(I_{OH} = -32mA)
Logic Low Output Level	V_{OL}		+0.2	+0.6	V	(I_{OL} = 32mA)
POWER						
Supply Voltage	V_{supply}	+4.9	+5.0	+5.1	V	
Supply Current	I_{supply}		67		mA	(both discriminators enabled)
Supply Current	I_{supply}		53		mA	(both discriminators disabled)
DIMENSIONS						
Width	W		84		mm	
Length	L		102		mm	(not including SMB connectors which extend past PCB edge)
Thickness	T		2.5		mm	(printed circuit board only)

Table 1: Specifications

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Typical Setup

A typical setup using a SIB164-1018 is shown below. A Hamamatsu H7546A MAPMT is mounted to the SIB164-1018 and positioned to detect incoming light from a scintillator crystal or optical assembly. The four anger logic outputs from the SIB164-1018 connect to four inputs on a PhotoniQ IQSP418 or IQSP518 multichannel PMT data acquisition system. Digitized output data from the PhotoniQ is sent through a USB 2.0 connection to a PC for display, logging, or real time processing. Additional connections between the SIB164-1018 and PhotoniQ provide a discriminator threshold adjustment signal to the SIB164-1018 and a trigger to the PhotoniQ from one of the SIB164-1018's three discriminators. When using an H7546A, a high voltage bias of up to negative 1000 volts is sent directly to the PMT from an SHV connector located on the rear of the PhotoniQ. Alternatively, bias to the PMT can be provided through the SIB164-1018 if an H7546B is used instead of an H7546A. Note that the rear panel high voltage output is an optional configuration on the IQSP418 and IQSP518.

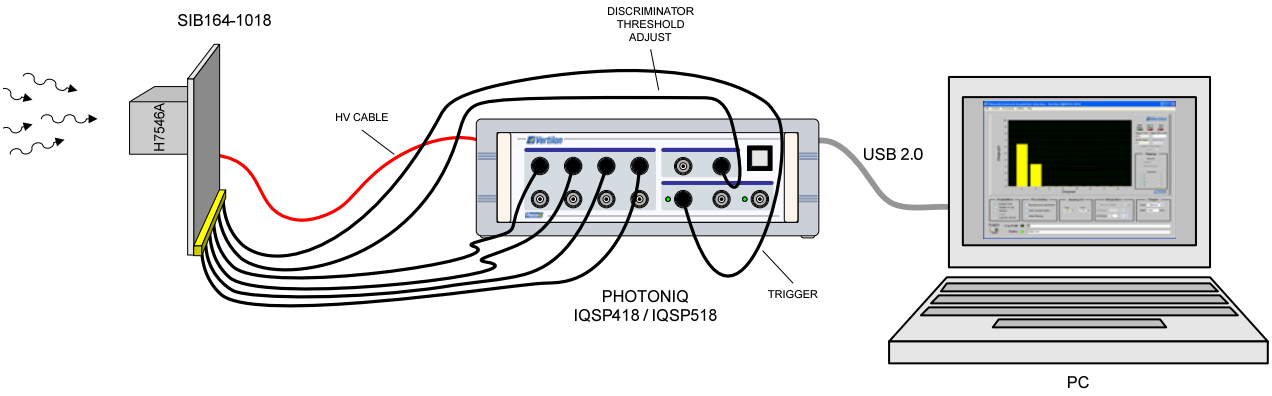


Figure 2: Typical Setup

High Voltage Interface

When using an H7546A, the high voltage cable from the PMT plugs directly into the SHV connector on the PhotoniQ. If an H7546B is used, the included socket pins should be installed on the SIB164-1018 so that a direct connection can be made between the PMT's bias voltage pins and the sensor interface board. In this configuration a specialized high voltage cable is used to supply the bias from the PhotoniQ to the proprietary high voltage connector on the SIB164-1018. In either configuration control of the PMT bias is accomplished through the PhotoniQ's graphical user interface. The SIB164-1018 employs the interface circuit shown below when the H7546B configuration is used.

Warning: The high voltage section of the SIB164-1018 contains signals at voltage levels that can exceed negative 1000 volts. Never touch a component or signal in this area.

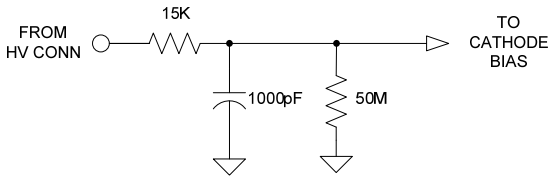


Figure 3: H7546B High Voltage Interface Circuit

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Photomultiplier Tube Anode Circuit

The 64 anode signals (P1 – P64) from the H7546 MAPMT are routed directly on the SIB164-1018 to the resistive anger logic circuit shown in the figure below. The four outputs labeled V1 to V4 are available on SMB connectors on the edge of the printed circuit board. These signals connect directly to a charge integrating data acquisition system like a Vertilon PhotoniQ IQSP418 or IQSP518. The PhotoniQ utilizes DC-coupled high speed transimpedance amplifiers that maintain a DC bias voltage of +0.250 volts on each of its inputs. For this reason it is important that all four outputs from the SIB164-1018 are directly connected to the PhotoniQ inputs — no additional interface circuitry is necessary.

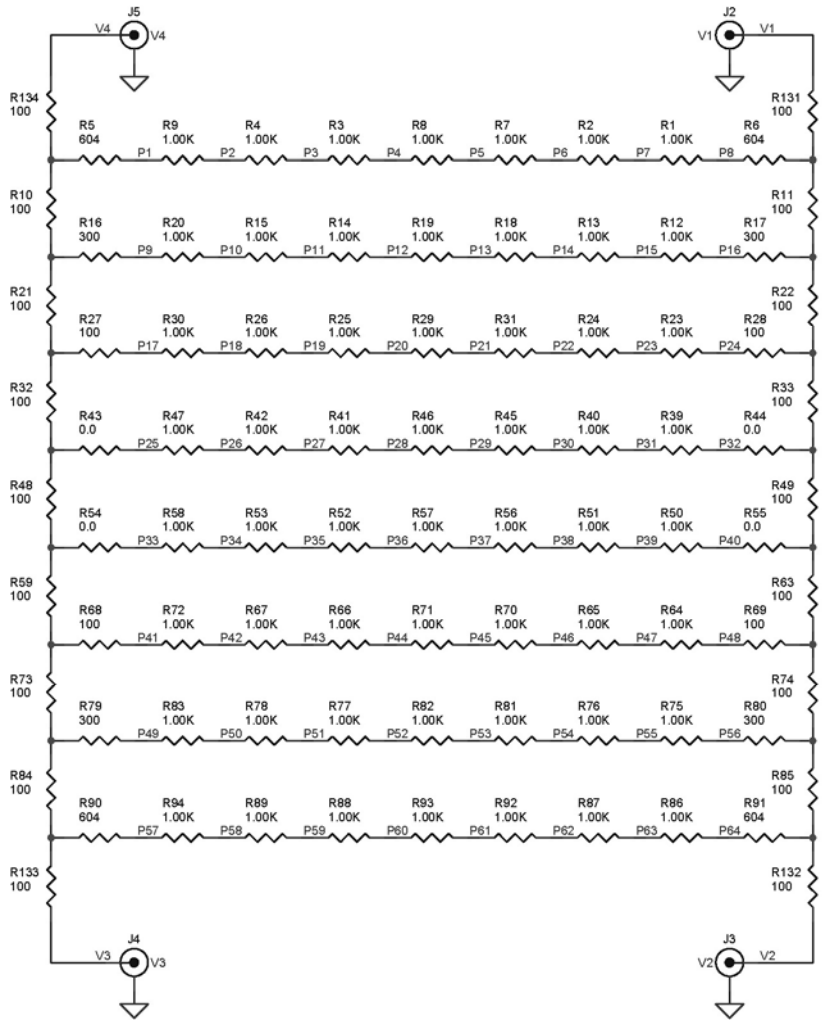


Figure 4: Resistive Anger Logic Circuit

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Last Dynode Output Preamplifier

This preamplifier is an inverting, AC-coupled, two-stage configuration designed for small positive voltage pulses from the last dynode output of the H7546. Connection of the PMT's last dynode output to the preamplifier is made at JP1 using a jumper. The preamplifier's output is further processed on the SIB164-1018 by three different discriminators to generate trigger signals synchronized with pulses on the last dynode output. For specialized applications requiring external discrimination of the last dynode signal, the preamplifier output is available on SMB connector, J6. When the preamplifier is not required, jumper JP1 should be left open.

Leading Edge Discriminator

The leading edge discriminator is a simple timing circuit that generates a trigger signal when a charge pulse on the last dynode output from the H7546 exceeds a user-defined threshold. It is implemented using a high speed comparator connected to the output of the last dynode output preamplifier. Referring to Figure 5, negative going pulses from the preamplifier are compared to a threshold that is adjusted using either the trimmer pot on the SIB164-1018 or an external DC voltage source. The adjustment method is selected with jumper JP4. When the trimmer pot is selected, the leading edge discriminator threshold is determined by the on-board potentiometer VR1 (LEAD). For the external control, the threshold is set though SMB connector J7 (DSCR ADJ) which normally connects to the front panel DAC on the PhotoniQ. Since the signal baseline for the SIB164-1018 discriminators is nominally +2.50V, the threshold should be adjusted slightly below this baseline voltage (see the specifications table for the scaling factor for the external threshold adjustment). A logic high is generated on the comparator output J8 (LEAD) after a small delay (t_{d1}) from when the pulse first crosses the threshold, V_{th1}. The comparator switches back to a logic low when the pulse crosses the threshold from the opposite direction as it returns back to the baseline level. Because the trigger point is sensitive to the pulse height, this discriminator is typically used in applications that do not require precision timing. When not used, the leading edge discriminator should be disabled by placing jumper JP7 into the left position.

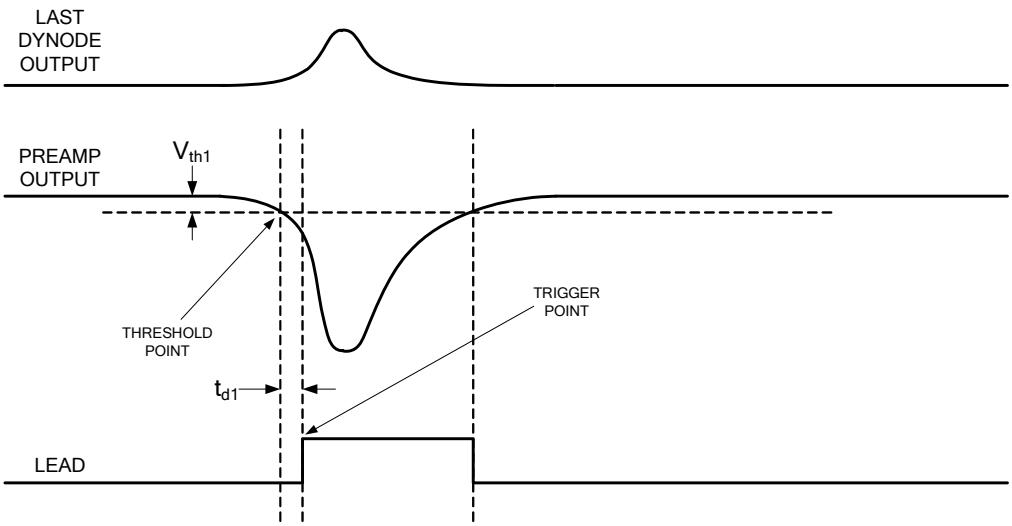


Figure 5: Leading Edge Discriminator Timing

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Constant Fraction Discriminator

Unlike leading edge discriminators, a constant fraction discriminator (CFD) is capable of generating precisely timed trigger signals that are relatively independent of input pulse height. The CFD accomplishes this by subtracting a fraction of the input from a delayed version of the input such that the resulting signal always crosses zero at exactly the same point in time. To minimize triggering on noise, the threshold is set just above the zero crossing point. The timing diagram in Figure 6 below illustrates the technique as implemented on the SIB164-1018. The CFD operates on the output of the last dynode preamplifier although technically only the delayed version of the signal (DELAY) is taken from the preamplifier output — the fractional part (FRACTION) is derived from the output of the first stage. The sum of these two components results in the AMP3 signal which is fed directly to the threshold comparator. This comparator, which to minimize noise triggering is only enabled when the output of the leading edge discriminator is high, compares AMP3 to a user-adjustable threshold voltage (V_{th2}) to generate the CFD output signal. By adjusting the delay time, fraction, and threshold (V_{th2}), the CFD can be made to trigger at a percentage of the pulse height maximum. Seven preset fractions from 0.12 to 0.50 are selectable using jumpers. The trigger threshold is adjusted using the external control signal DSCR ADJ on connector J7. Like the threshold control for the leading edge discriminator, this signal is generated by the DAC output from the PhotoniQ front panel and the baseline level is +2.50V. The threshold however is adjusted positively with respect to this level. To use the CFD, jumper JP11 is placed in the upper position and the leading edge discriminator is enabled. The threshold control for the leading edge discriminator must be set to the trimmer pot since the CFD threshold can only be set by the DSCR ADJ signal.

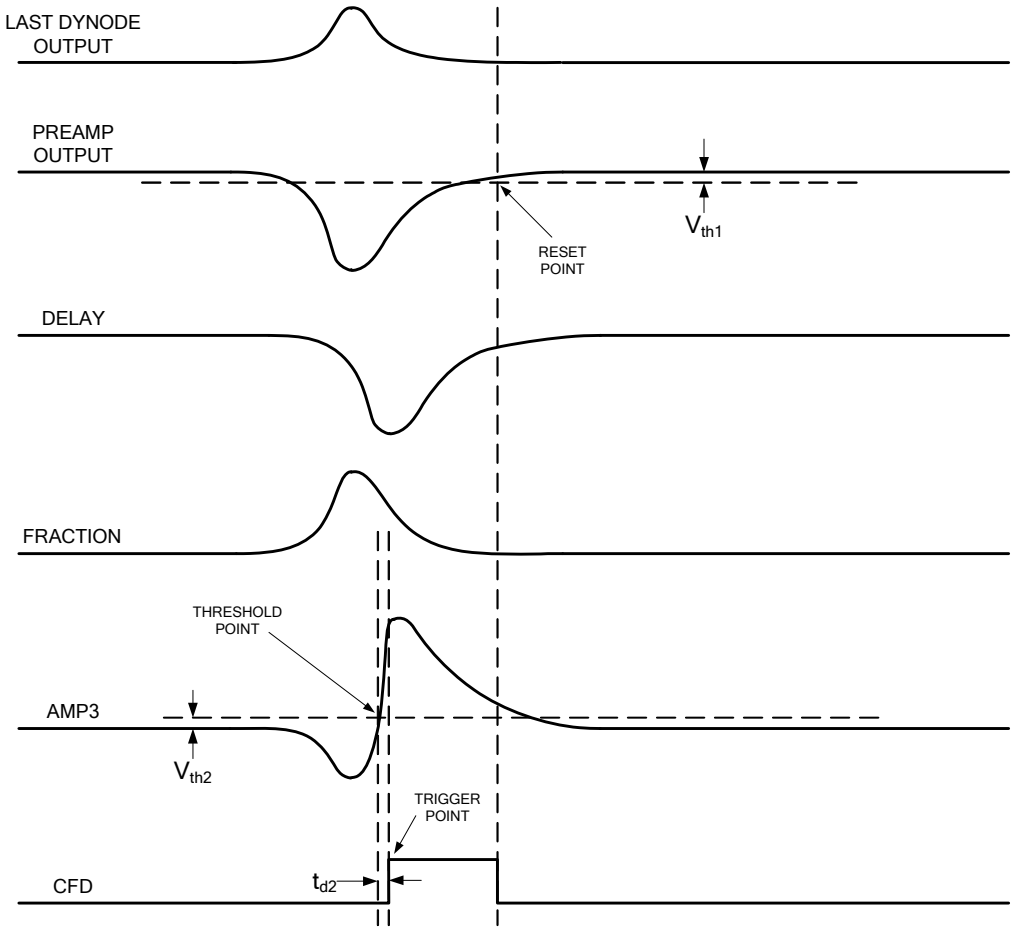


Figure 6: Constant Fraction Discriminator Timing

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Zero Slope Discriminator

The zero slope discriminator (ZSD) works by generating a trigger signal at the inflection point of the input pulse. It is at this point where the pulse is at its peak and its slope transitions from positive to negative. Since AMP4 effectively operates on the derivative of the input pulse, its output crosses zero where the slope of the pulse is zero. This occurs at the *threshold point* shown in Figure 7. The threshold comparator compares AMP4 to the user-adjustable threshold (V_{th3}) to generate the trigger signal. Similar to the constant fraction discriminator, the threshold for the zero slope discriminator is referenced to +2.50V and controlled by the PhotoniQ DAC signal fed into DSCR ADJ on connector J7. The zero slope discriminator is selected by placing jumper JP11 into the lower position and enabling the leading edge discriminator. Jumper JP8 is used to disable both the zero slope and constant fraction discriminators by inserting it into the left position.

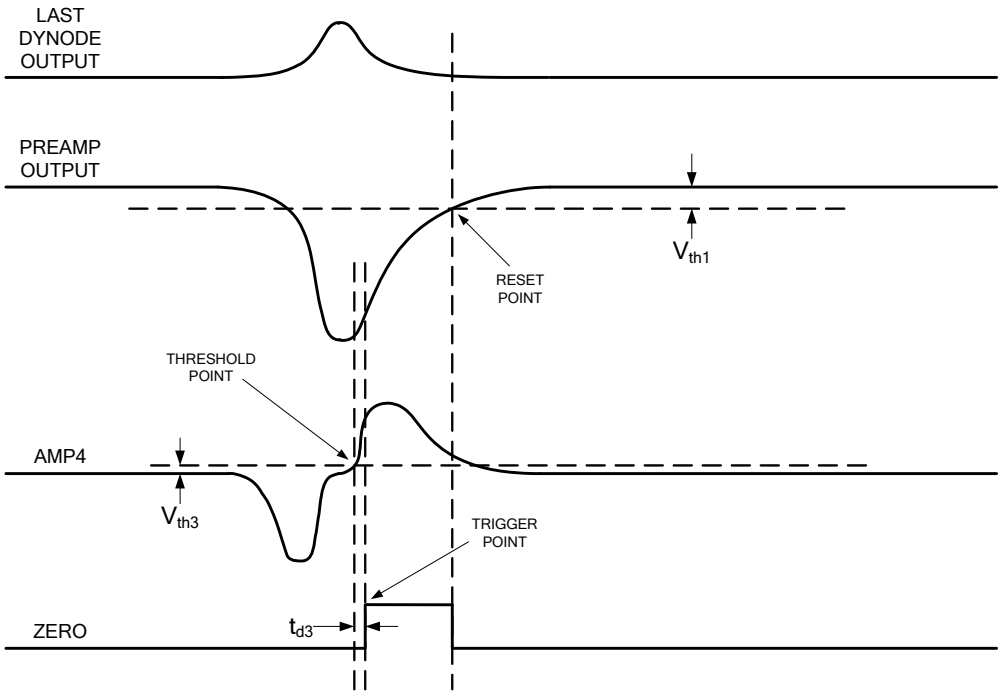


Figure 7: Zero Slope Discriminator Timing

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Top and Bottom Views

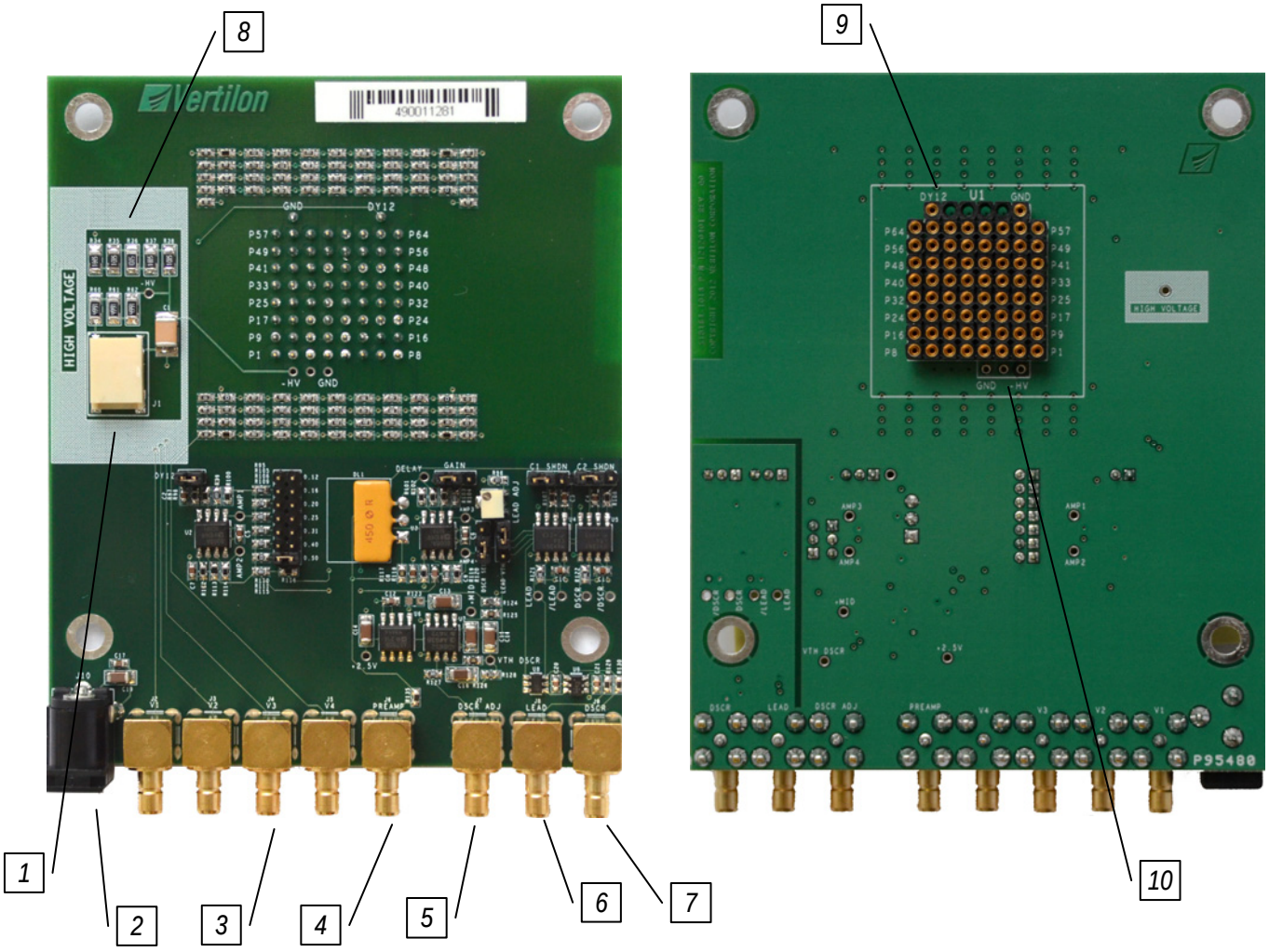


Figure 8: Top and Bottom Views

1. High Voltage Input (J1)
2. +5V Power Input (J10)
3. Anger Logic Outputs (J2 – J5)
4. Last Dynode Preamp Output (J6)
5. Discriminator Threshold Adjustment (J7)
6. Leading Edge Discriminator Output (J8)
7. CFD / ZSD Discriminator Output (J9)
8. MAPMT High Voltage Bias Circuit
9. H7546 Anode & Dynode Connectors
10. H7546B High Voltage Connector

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Component Locations and Functions

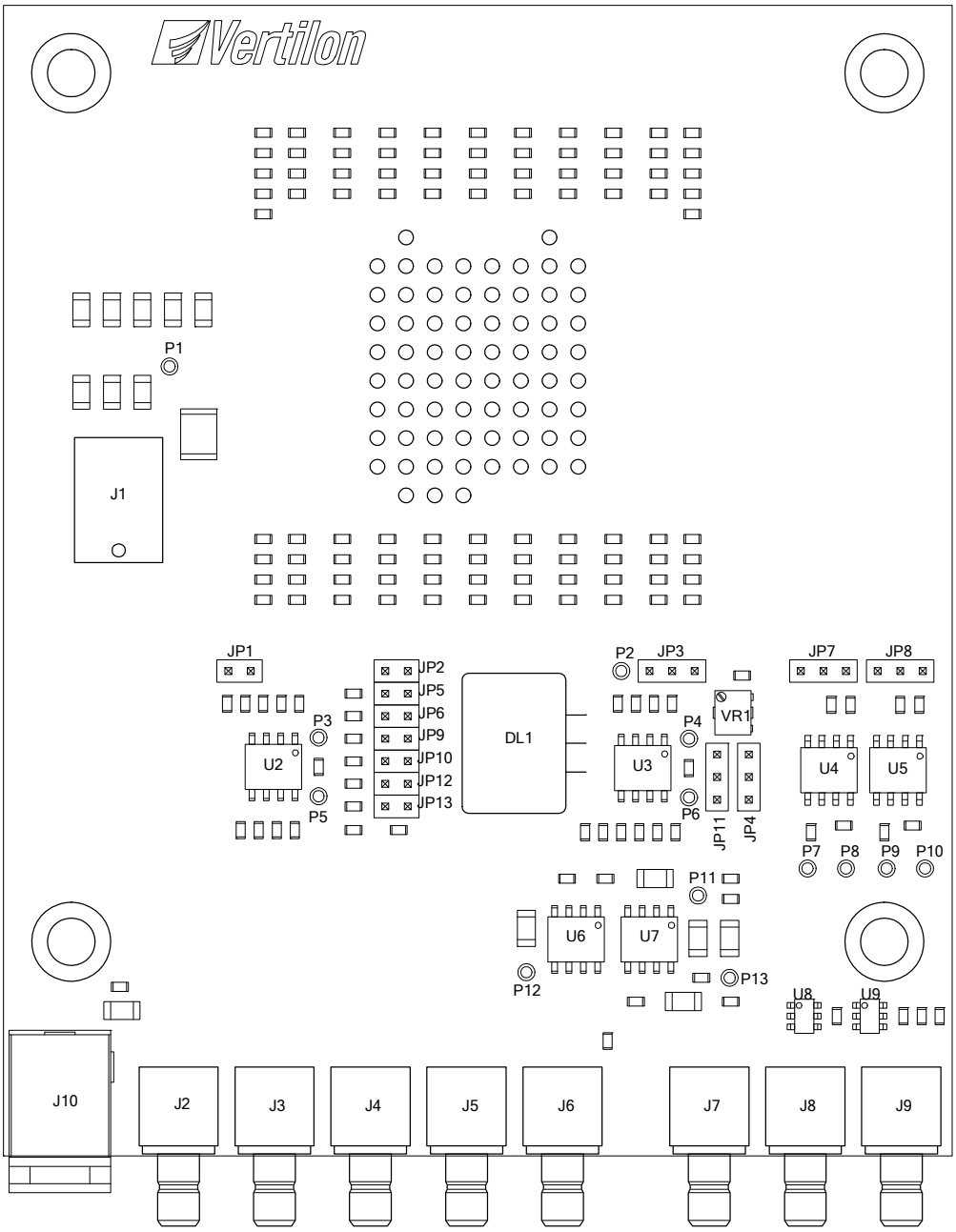


Figure 9: Component Locations and Functions

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Name	Function	Description
J1	-HV	Optional negative high voltage bias input
J2	V1	Anger logic V1 output, anode P8
J3	V2	Anger logic V2 output, anode P64
J4	V3	Anger logic V3 output, anode P57
J5	V4	Anger logic V4 output, anode P1
J6	PREAMP	Last dynode preamplifier output
J7	DSCR ADJ	Threshold adjustment input for discriminators
J8	LEAD	Leading edge discriminator output
J9	DSCR	Constant fraction / zero slope discriminator output
J10	POWER	Power supply input, +5V

Table 2: Connectors

Name	Function	Description
JP1	DY12	Last dynode jumper to preamplifier
JP3	GAIN	Constant fraction discriminator gain (left position = highest gain)
JP4	LEAD VTH	Select for leading edge discriminator threshold input (upper position = potentiometer, lower position = external)
JP11	DSCR SEL	Discriminator select (upper position = CFD, lower position = ZSD)
JP2, JP5, JP6, JP9, JP10, JP12, JP13	CFD FRACTION	CFD fraction: 0.12, 0.16, 0.20, 0.25, 0.31, 0.40, 0.50 JP2 = minimum, JP13 = maximum
JP7	C1 SHDN	Power to leading edge discriminator (left position = disabled)
JP8	C2 SHDN	Power to CFD and ZSD discriminators (left position = disabled)

Table 3: Jumpers

Name	Ref #	Description
-HV	P1	MAPMT cathode bias. Warning: This is a high voltage point that can exceed negative 1000 volts.
DELAY	P2	Output of constant fraction discriminator delay path. Reference to AMP2 to measure the delay.
AMP1	P3	Output of amplifier #1 of last dynode output signal processing chain.
AMP3	P4	Output of amplifier #3 of constant fraction discriminator.
AMP2	P5	Output of amplifier #2 of last dynode output signal processing chain.
AMP4	P6	Output of amplifier #4 of zero slope discriminator.
LEAD	P7, P8	Leading edge discriminator comparator output, positive (+) and negative (-).
DSCR	P9, P10	Constant fraction / zero slope discriminator comparator output, positive (+) and negative (-).
+MID	P11	Baseline voltage for last dynode output signal processing chain. Nominally +2.5V.
+2.5V	P12	+2.5V reference voltage
VTH DSCR	P13	Threshold for constant fraction / zero slope discriminator.

Table 4: Test Points

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Mechanical Information

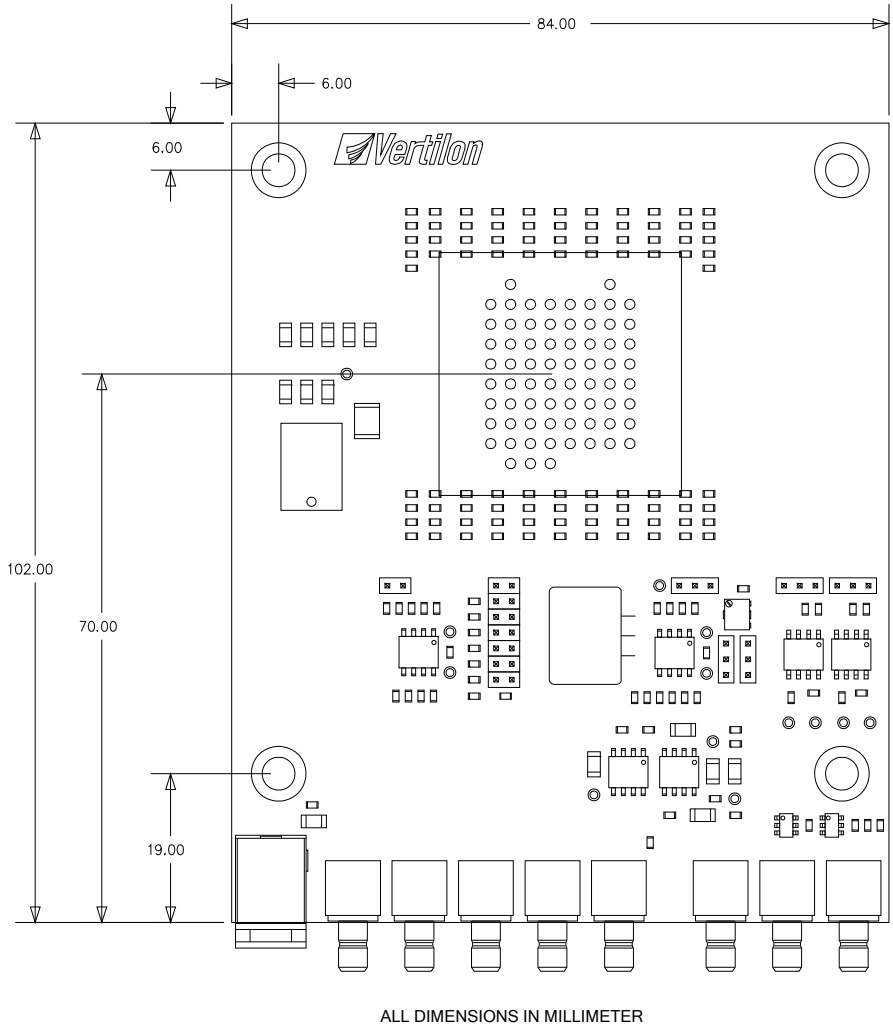


Figure 10: SIB164-1018 Printed Circuit Board Dimensions

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

UG2859.1.0 Dec 2012

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com