User Guide

SIB264
64 Channel MCP-PMT Interface Board
Photonis XP85013 series

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

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General Safety Precautions

Use Proper Power Source

The SIB264 is powered with a +5V power source directly from Vertilon's PhotoniQ multi-channel data acquisition systems. Use with any other power source may result in damage to the product.

Operate Inputs within Specified Range

To avoid electric shock, fire hazard, or damage to the product, do not apply a voltage to any input outside of its specified range.

Electrostatic Discharge Sensitive

Electrostatic discharges may result in damage to the SIB264. For these reasons, the SIB264 board is intended to be operated in a user's conductive instrument enclosure.

Do Not Operate in Wet or Damp Conditions

To avoid electric shock or damage to the product, do not operate in wet or damp conditions.

Do Not Operate in Explosive Atmosphere

To avoid injury or fire hazard, do not operate in an explosive atmosphere.

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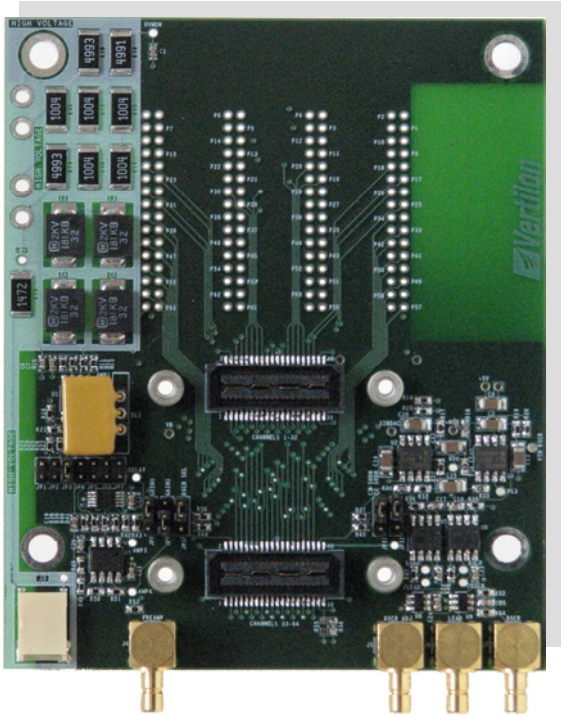
Product Overview



- Mounting board for Photonis XP85013 64 channel MCP-PMT
- Provides 64 channel interface to data acquisition systems
- Separate high voltage input for MCP-PMT cathode bias
- High speed preamplifier for microchannel plate output
- Leading edge, constant fraction, and zero slope discriminators
- Adjustable gain and discriminator thresholds
- 100% compatible with Vertilon's PhotoniQ multichannel DAQs
- No external power supply required

The SIB264 multianode photomultiplier tube interface board provides the mechanical and electrical connectivity between the Photonis XP85013 series 64 anode MCP-PMT and external signal processing electronics such as Vertilon's PhotoniQ multichannel data acquisition systems. The XP85013 is mounted to the bottom side of the SIB264 through 128 socket pins that connect the MCP-PMT's 64 anode signals to the board. The anode signals are routed to two connectors located on the top of the board that each connect to a specialized high density coaxial cable assembly. This arrangement allows the SIB264 to be conveniently mounted directly into the user's optical setup with the MCP-PMT facing outward from the bottom of the board and the sensor interface board (SIB) cables exiting from the top. The SIB cables carry the 64 anodes from the XP85013 to the PhotoniQ where the charge from each is separately integrated, digitized, and sent to a PC for display or further signal processing. The negative high voltage bias to the MCP-PMT's cathode is supplied directly from the PhotoniQ on a high voltage cable to a dedicated connector on the SIB264. This voltage is used by an on-board bias generator circuit to derive the required high voltages for the XP85013's microchannel plate. For applications requiring timing pickoff from the XP85013, the SIB264 includes a two stage high speed preamplifier for the microchannel plate output and three types of pulse discriminators. The outputs from a leading edge, constant fraction, and zero slope discriminator respectively generate trigger signals based on a threshold, percentage of pulse height, and pulse peak. These outputs as well as the preamplifier output are available to the user for connection to the PhotoniQ or other external electronics. Several user adjustments are included for optimizing system gain and trigger thresholds for the discriminators.

The various functions on the SIB264 are described in greater detail on the following pages. When necessary, refer to the functional block diagram shown in Figure 1 below.

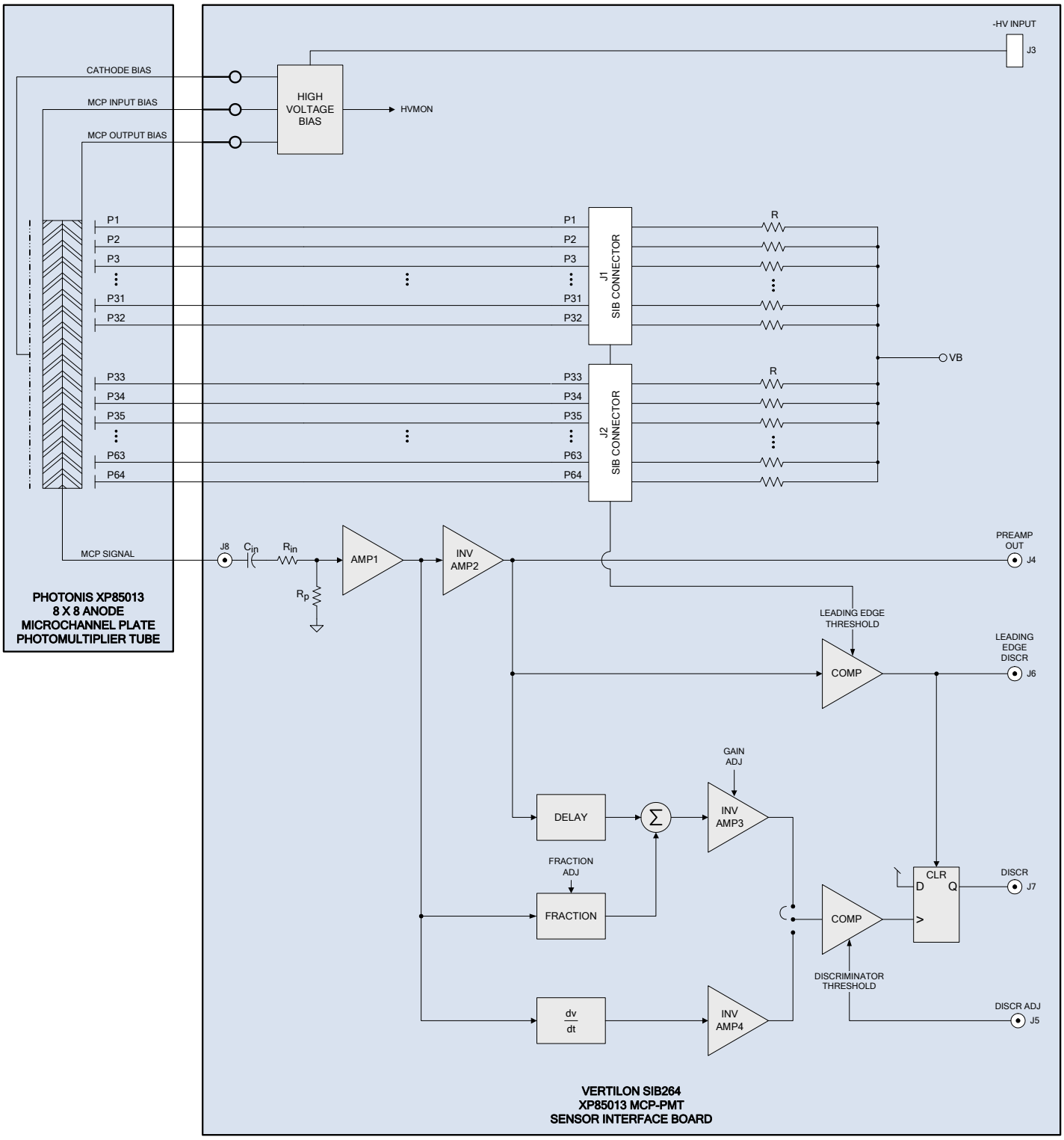


Figure 1: Functional Block Diagram

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Specifications

(V_{supply} = +5.0V, T_A = +25C, unless otherwise noted)

Description	Sym	Min	Typ	Max	Units	Notes
HIGH VOLTAGE						
High Voltage Input Load Resistance			6		MΩ	Measured at high voltage input connector, J3
HVMON to High Voltage Input Ratio			0.00083			±10%
ANODE CIRCUITS						
Quantity	P1 - P64		64			
Input Resistance	R		2.2		MΩ	
Input Bias Voltage	VB		+0.250		V	Detector bias voltage supplied from PhotoniQ data acquisition system
MCP SIGNAL PREAMPLIFIER						
Input Coupling Capacitance	C_{in}		0.1		uF	
Input Resistance	R_{in}		50		Ω	
Input Parallel Resistance	R_p		500		Ω	
Amplifier #1 Gain	A1		12.6		dB	
Amplifier #2 Inverting Gain	A2		6		dB	V_{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to input (J8).
Amplifier #2 Output Impedance			50		Ω	Measured at preamplifier output, J4
LEADING EDGE DISCRIMINATOR						
Threshold Adjustment	V_{th1}	-50		0	mV	Referenced to baseline level at comparator input. Maximum threshold occurs when PhotoniQ SIB DAC = +3.00V.
Threshold to Output Delay (V_{in}=30mV)	t_{d1}		5		nsec	
Time Walk (V_{in}: 3mV to 30mV)			-13		nsec	Output on connector, J6.
Time Walk (V_{in}: 30mV to 150mV)			-3.0		nsec	V_{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to preamplifier input (J8). Threshold (V_{th1}) set to 15mV below the baseline.
Jitter (V_{in}: 10mV)			1		nsec	
CONSTANT FRACTION DISCRIMINATOR						
Delay	D		6		nsec	Standard delay element, other delays available.
Delay to Fraction Ratio		0.12		0.50		7 steps of 2 dB each Steps: 0.12, 0.16, 0.20, 0.25, 0.31, 0.40, 0.50
Amplifier #3 Inverting Gain	A3		+8.6		dB	
Threshold Adjustment	V_{th2}	0		+50	mV	Referenced to baseline level at comparator input. Maximum threshold occurs when PhotoniQ front panel DAC = +3.00V
Threshold to Output Delay (V_{in}=30mV)	t_{d2}		5		nsec	Output on connector, J7.
Time Walk (V_{in}: 20mV to 100mV)			-2.0		nsec	V_{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to preamplifier input (J8). Threshold (V_{th2}) set to 15mV above the baseline. Fraction set to 0.50.
Jitter (V_{in}: 50mV)			500		psec	

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Description	Sym	Min	Typ	Max	Units	Notes
ZERO SLOPE DISCRIMINATOR						
Differentiator First-Order Time Constant			3.3		nsec	
Amplifier #4 Inverting Gain	A4		10.4		dB	
Threshold Adjustment	V_{th3}	0		+50	mV	Referenced to baseline level at comparator input. Maximum threshold occurs when PhotoniQ front panel DAC = +3.00V
Threshold to Output Delay (V_{in}=30mV)	t_{d3}		5		nsec	Output on connector, J7.
Time Walk (V_{in}: 20mV to 150mV)			-3.0		nsec	V_{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to preamplifier input (J8). Threshold (V_{th3}) set to 5mV above the baseline.
Jitter (V_{in}: 100mV)			500		psec	
DISCRIMINATOR OUTPUTS						
Output Impedance			50		Ω	
Logic High Output Level	V_{OH}	+4.3	+4.8		V	(I_{OH} = -32mA)
Logic Low Output Level	V_{OL}		+0.2	+0.6	V	(I_{OL} = 32mA)
POWER						
Supply Voltage	V_{supply}	+4.9	+5.0	+5.1	V	
Supply Current	I_{supply}		75		mA	(both comparators enabled)
Supply Current	I_{supply}		60		mA	(both comparators disabled)
DIMENSIONS						
Width	W		84		mm	
Length	L		102		mm	(not including SMB connectors which extend past PCB edge)
Thickness	T		2.5		mm	(printed circuit board only)

Table 1: Specifications

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Typical Setup

A typical setup using a SIB264 is shown below. The Photonis XP85013 MCP-PMT is mounted to the SIB264 and positioned to detect incoming light from a scintillator crystal or optical assembly. Two SIB cables connect the 64 anode outputs from the SIB264 to a PhotoniQ IQSP482 or IQSP582 64 channel PMT data acquisition system. Digitized output data from the PhotoniQ is sent through a USB 2.0 connection to a PC for display, logging, or real time processing. Additional connections between the SIB264 and PhotoniQ provide a high voltage of up to negative 1500 volts to bias the XP85013 cathode and MCP, a discriminator threshold adjustment signal to the SIB264, and a trigger to the PhotoniQ from one of the SIB264's three discriminators. In an alternative configuration when precision timing is required, an external discriminator can be placed between the SIB264 preamplifier output and the PhotoniQ trigger input.

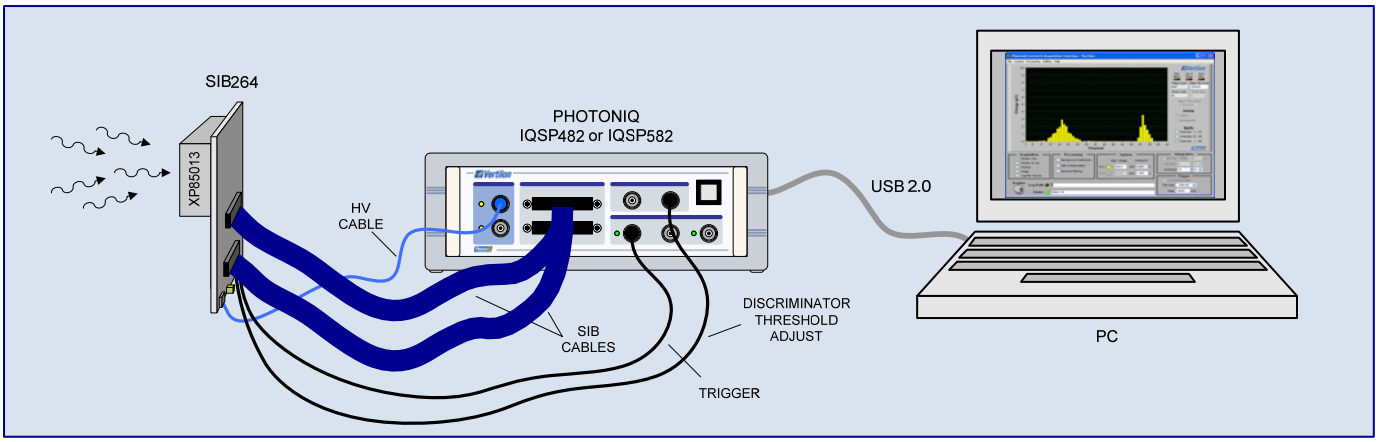

Figure 2: Typical Setup

High Voltage Interface

The SIB264 employs the interface circuit shown below between the high voltage input connector, J3, and the high voltage bias inputs to the XP85013. When using the on-board bias generator, the flying leads from the XP85013 should be soldered directly to their corresponding points on the SIB264. The monitor output (HVMON) allows the high voltage cathode bias for the MCP-PMT to be indirectly monitored at a reduced voltage level. Voltage readings at the monitor point should be scaled by a factor of 1200. Calibration of the scale factor may be required.

Warning: The high voltage section of the SIB264 contains signals at voltage levels that can exceed negative 2500 volts. Never touch a component or signal in this area.

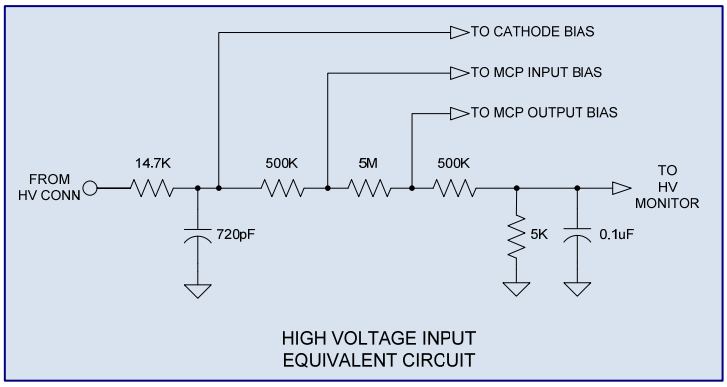

Figure 3: MCP-PMT High Voltage Interface Circuit

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Microchannel Plate Photomultiplier Tube Anode Circuits

The 64 anode signals (P1 – P64) from the XP85013 MCP-PMT are routed directly on the SIB264 to two specialized connectors referred to as sensor interface board (SIB) connectors. Anodes P1 to P32 route to SIB connector J1 and anodes P33 to P64 route to SIB connector J2. Each SIB connector mates to a proprietary low-noise, high density SIB cable assembly that carries the 32 anode signals on coaxial connections to a Vertilon PhotoniQ 64 channel PMT data acquisition system. Depending on the required speed and dynamic range, either a PhotoniQ IQSP482 high dynamic range system or an IQSP582 high speed system can be used as the main data acquisition unit. To minimize the possibility of damage due to ESD, the XP85013 anodes each have a 2.2 Mohm shunt resistor to a common low impedance point. This point is biased at a voltage equal to the bias voltage (VB) of the charge integrating transimpedance amplifiers on the PhotoniQ so that the anodes can be DC coupled to the amplifiers. Figure 4 below illustrates the equivalent circuit as seen by each MCP-PMT anode.

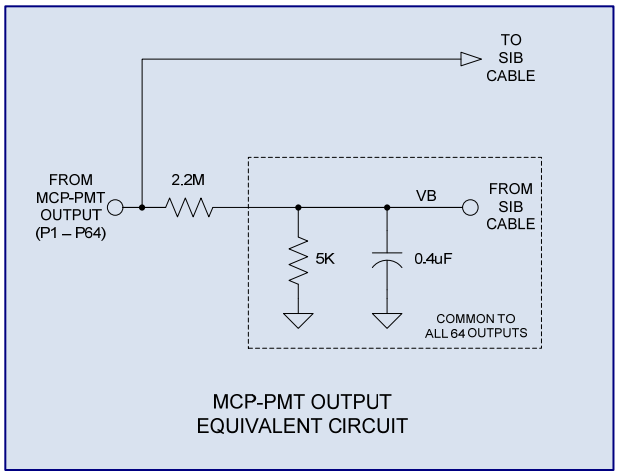

Figure 4: Anode Circuit

Microchannel Plate Output Preamplifier

This preamplifier is an inverting, AC-coupled, two-stage configuration designed for small positive voltage pulses from the microchannel plate of the XP85013. Connection to the preamplifier is made at connector J8 using a miniature MMCX coaxial connector attached to the RG178 B/U coaxial cable output from the XP85013. The preamplifier's output is further processed on the SIB264 by three different discriminators to generate trigger signals in sync with a pulse on the MCP output. For specialized applications requiring external discrimination of the MCP signal, the preamplifier output is available on SMB connector, J4. When the preamplifier is not required, connector J8 should be left open.

Leading Edge Discriminator

The leading edge discriminator is a simple timing circuit that generates a trigger signal when a charge pulse on the MCP output from the XP85013 exceeds a user-defined threshold. It is implemented using a high speed comparator connected to the output of the MCP output preamplifier. Referring to Figure 5, negative going pulses from the preamplifier are compared to a threshold that is adjusted using the sensor interface board DAC (SIB DAC) accessible through the PhotoniQ GUI. Since the signal baseline for the SIB264 discriminators is nominally +2.5V, the threshold should be adjusted slightly below this baseline voltage. The SIB DAC should be adjusted between +2.50V (0mV threshold) and +3.00V (50mV threshold). A logic high is generated on the comparator output (SMB connector, J6) after a small delay (t_{d1}) from when the pulse first crosses the threshold, V_{th1}. The comparator switches back to a logic low when the pulse

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crosses the threshold from the opposite direction as it returns back to the baseline level. Because the trigger point is sensitive to the pulse height, this discriminator is typically used in applications that do not require precision timing. When not used, the leading edge discriminator should be disabled by placing jumper JP12 into the upper position.

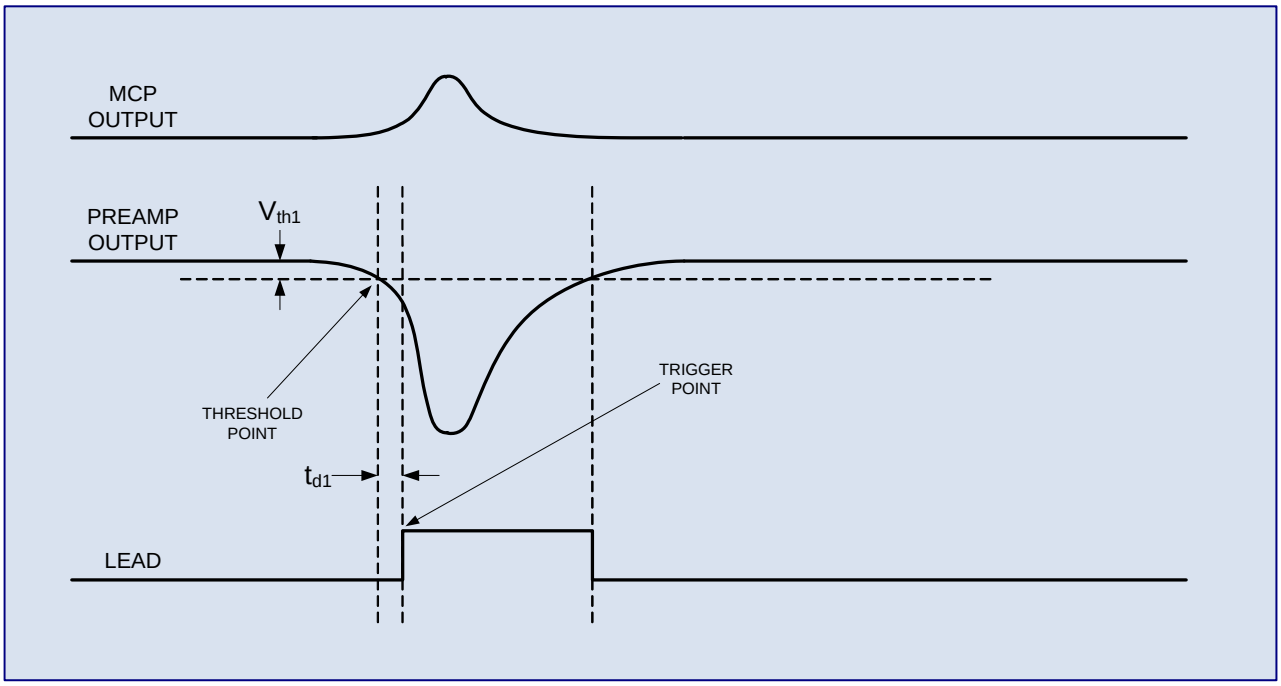

Figure 5: Leading Edge Discriminator Timing

Constant Fraction Discriminator

Unlike leading edge discriminators, a constant fraction discriminator (CFD) is capable of generating precisely timed trigger signals that are relatively independent of input pulse height. The CFD accomplishes this by subtracting a fraction of the input from a delayed version of the input such that the resulting signal always crosses zero at exactly the same point in time. To minimize triggering on noise, the threshold is set just above the zero crossing point. The timing diagram in Figure 6 below illustrates the technique as implemented on the SIB264. The CFD operates on the output of the MCP output preamplifier although technically only the delayed version of the signal (DELAY) is taken from the preamplifier output — the fractional part (FRACTION) is derived from the output of the first stage. The sum of these two components results in the AMP3 signal which is fed directly to the threshold comparator. This comparator, which to minimize noise triggering is only enabled when the output of the leading edge discriminator is high, compares AMP3 to a user-adjustable threshold voltage (V_{th2}) to generate the CFD output signal. By adjusting the delay time, fraction, and threshold (V_{th2}), the CFD can be made to trigger at any reasonable percentage of the pulse height maximum. Seven preset fractions from 0.12 to 0.50 that are selectable using jumpers JP1 to JP7, respectively. The trigger threshold is adjusted using an external control signal fed through SMB connector J5. Typically this signal is generated by the DAC output from the PhotoniQ front panel and like the threshold control for the leading edge discriminator, the baseline level is +2.5V. The threshold however is adjusted positively with respect to this level. The PhotoniQ front panel DAC should be adjusted between +2.50V (0mV threshold) and +3.00V (50mV threshold). The SIB264 ships with a standard fixed delay of 6 nsec — other delays of up to 10 nsec can be ordered separately. To use the CFD, jumper JP10 is placed into the upper position and the leading edge discriminator is enabled.

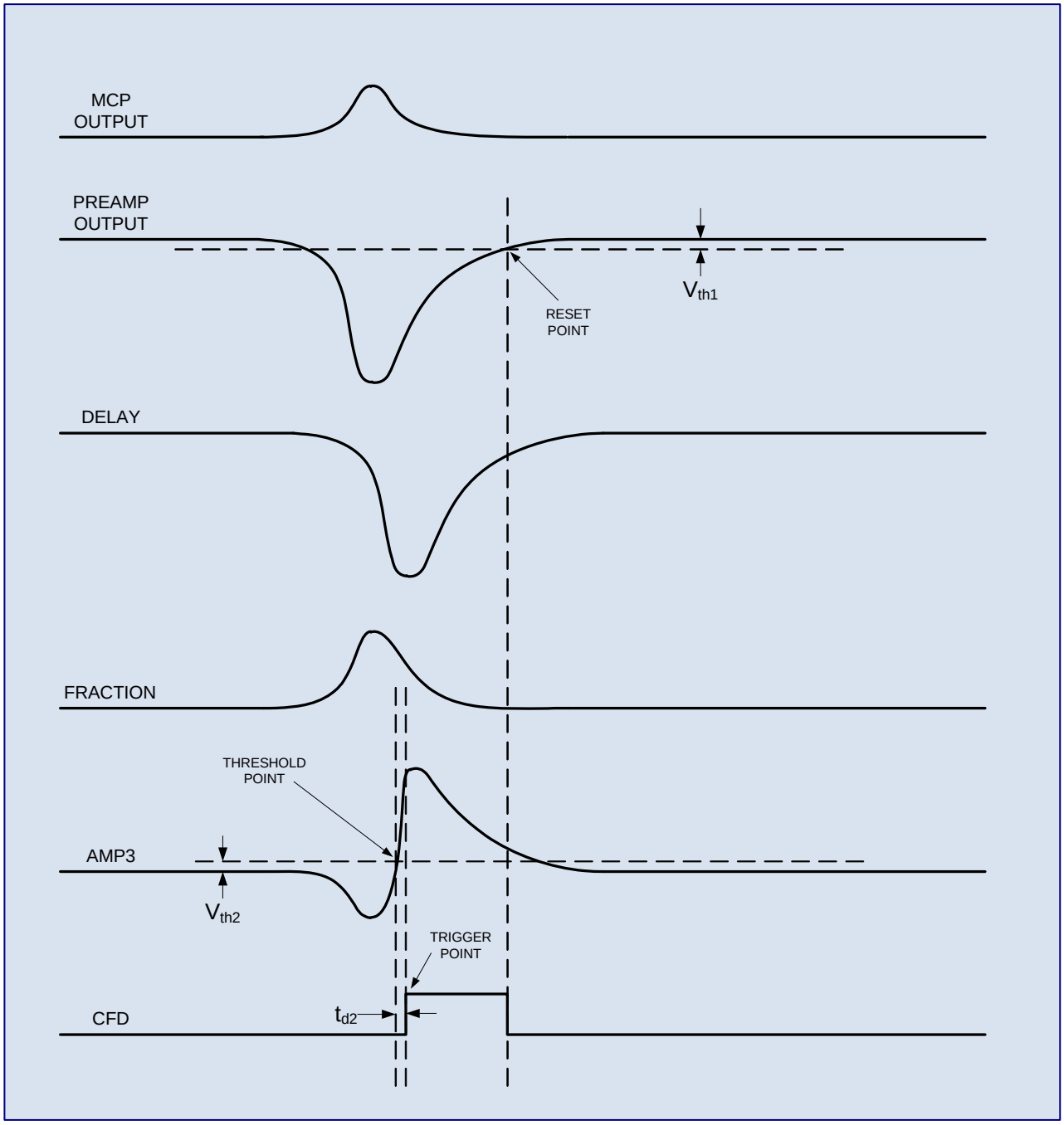

Figure 6: Constant Fraction Discriminator Timing

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Zero Slope Discriminator

The zero slope discriminator (ZSD) works by generating a trigger signal at the inflection point of the input pulse. It is at this point where the pulse is at its peak and its slope transitions from positive to negative. Since AMP4 effectively operates on the derivative of the input pulse, its output crosses zero where the slope of the pulse is zero. This occurs at the *threshold point* shown in Figure 7. The threshold comparator compares AMP4 to the user-adjustable threshold (V_{th3}) to generate the trigger signal. Similar to the constant fraction discriminator, the threshold for the zero slope discriminator is referenced to +2.5V and controlled by the PhotoniQ front panel DAC signal fed into SMB connector J5. The zero slope discriminator is selected by placing jumper JP10 into the lower position and enabling the leading edge discriminator. Jumper JP11 is used to disable both the zero slope and constant fraction discriminators by inserting it into the upper position.

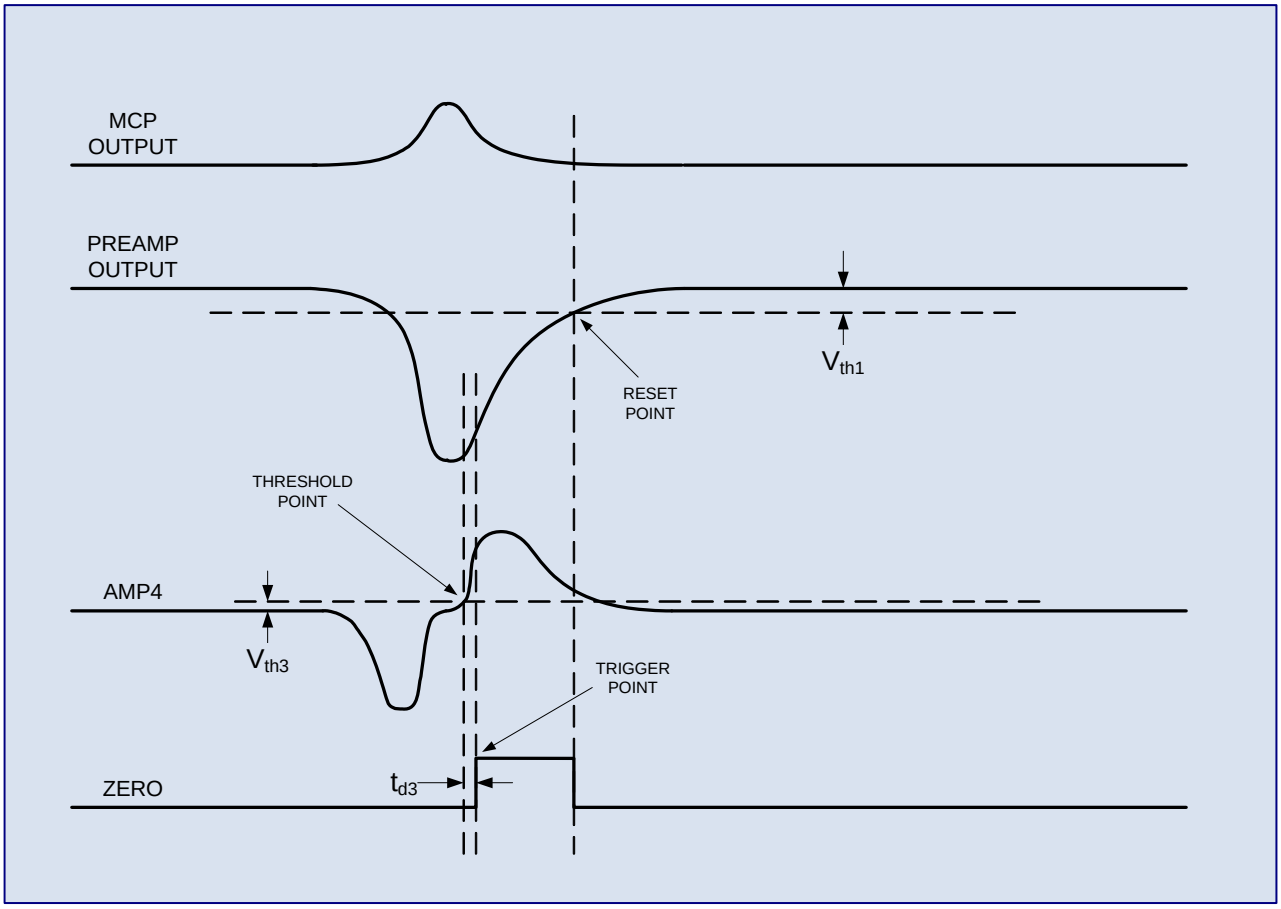

Figure 7: Zero Slope Discriminator Timing

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Top and Bottom Views

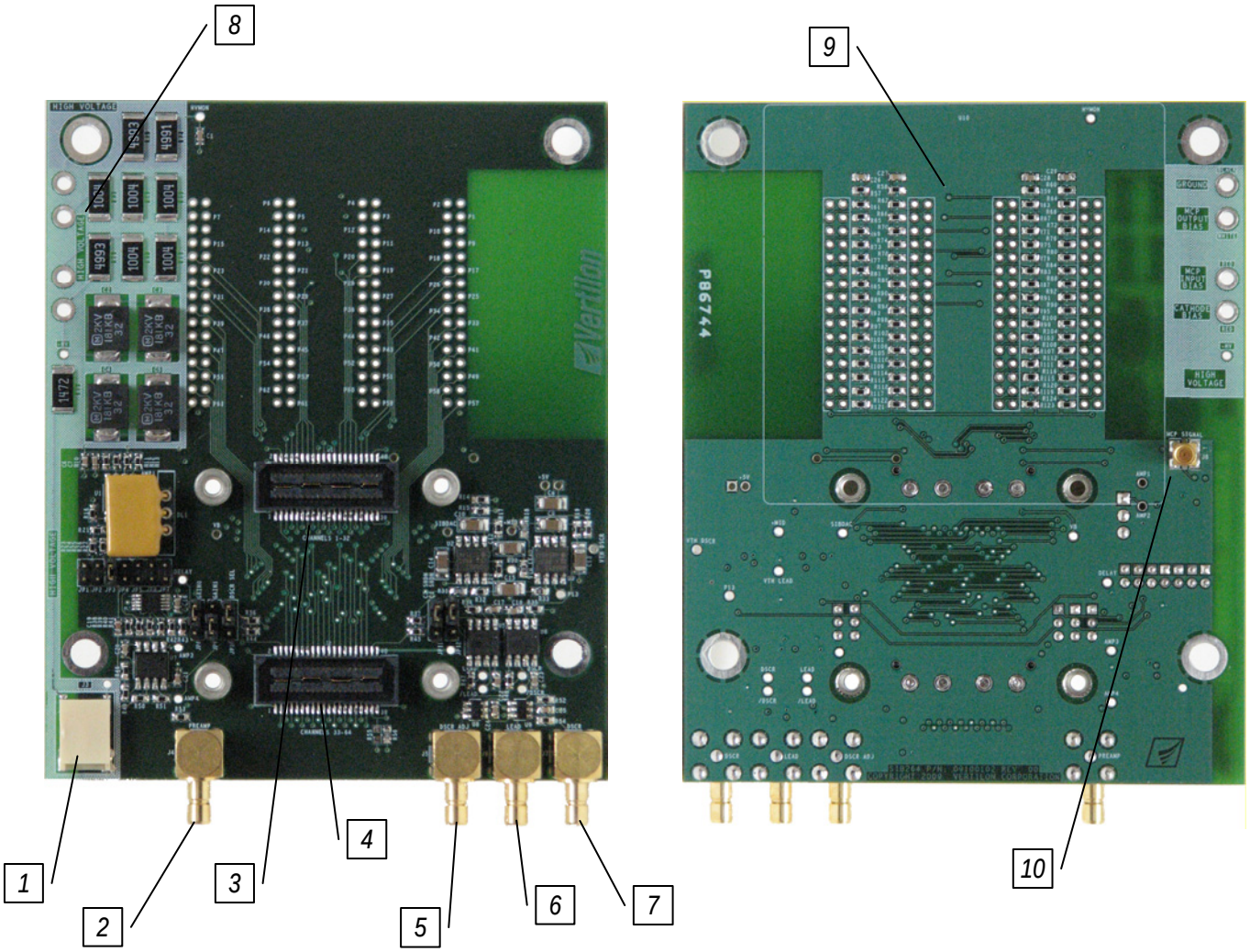

Figure 8: Top and Bottom Views

1. High Voltage Input (J3)
2. MCP Preamp Output (J4)
3. Sensor Interface Board Connector (J1)
4. Sensor Interface Board Connector (J2)
5. Discriminator Threshold Adjustment (J5)
6. Leading Edge Discriminator Output (J6)
7. CFD / ZSD Discriminator Output (J7)
8. MCP-PMT High Voltage Bias Connections
9. XP85013 Socket Connectors
10. XP85013 MCP Output Connector (J8)

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Component Locations and Functions

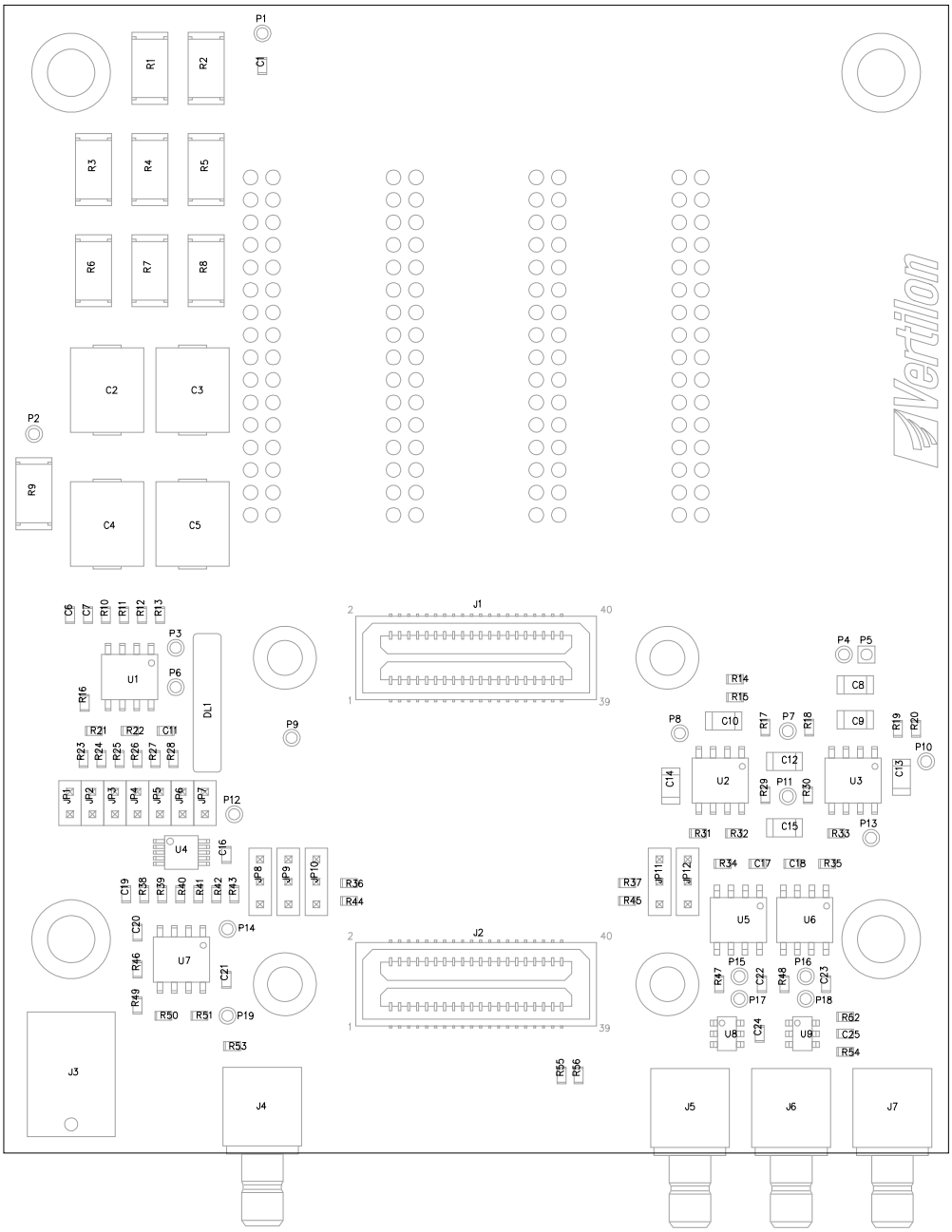

Figure 9: Component Locations and Functions

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Name	Function	Description
J1	CHANNELS 1 - 32	Sensor interface board connector to SIB cable for channels 1 -32
J2	CHANNELS 33 - 64	Sensor interface board connector to SIB cable for channels 33 - 64
J3	-HV	Negative high voltage bias input
J4	PREAMP	MCP preamplifier output
J5	DSCR ADJ	Threshold adjustment input for the constant fraction / zero slope discriminators
J6	LEAD	Leading edge discriminator output
J7	DSCR	Constant fraction / zero slope discriminator output

Table 2: Connectors

Name	Function	Description
JP1 – JP7	CFD FRACTION	CFD fraction: 0.12, 0.16, 0.20, 0.25, 0.31, 0.40, 0.50 (JP1 = minimum, JP7 = maximum)
JP8	GAIN0	Constant fraction discriminator gain LSB (upper position = highest gain)
JP9	GAIN1	Constant fraction discriminator gain MSB (upper position = highest gain)
JP10	DSCR SEL	Discriminator select. (upper position = CFD, lower position = ZSD)
JP11	C2 SHDN	Power to CFD and ZSD discriminators: (upper position = disabled)
JP12	C1 SHDN	Power to leading edge discriminator: (upper position = disabled)
DL1	DELAY	Programmable delay element for constant fraction discriminator

Table 3: Jumpers

Name	Description
+5V	Main +5V power to the SIB264 supplied by the PhotoniQ through SIB connectors J1 and J2.
VB	Anode bias and reference voltage to the SIB264 supplied by the PhotoniQ through SIB connectors J1 and J2.
+MID	Baseline voltage for MCP output signal processing chain. Nominally +2.5V.
-HV	MCP-PMT cathode bias. Warning: This is a high voltage point that can exceed negative 2500 volts.
HVMON	Highly attenuated version of –HV used for indirectly monitoring MCP-PMT cathode bias.
AMP1	Output of amplifier #1 of MCP output signal processing chain.
AMP2	Output of amplifier #2 of MCP output signal processing chain.
AMP3	Output of amplifier #3 of constant fraction discriminator.
AMP4	Output of amplifier #4 of zero slope discriminator.
DELAY	Output of constant fraction discriminator delay path. Reference to AMP2 to measure the delay.
LEAD	Leading edge discriminator comparator output, positive (+) and negative (-).
DSCR	Constant fraction / zero slope discriminator comparator output, positive (+) and negative (-).
VTH LEAD	Threshold for leading edge discriminator.
VTH DSCR	Threshold for constant fraction / zero slope discriminator.
SIBDAC	Digital to analog converter output from PhotoniQ to sensor interface board.
P13	Reserved signal.

Table 4: Test Points

SIB Connector Pinout

The SIB264 connectors and cables are fully compatible with all Vertilon PhotoniQ systems. For applications utilizing data acquisition systems other than Vertilon's PhotoniQ series, the pinout for connectors J1 and J2 is provided in Table 5 as a reference.

SIB Connector J1					
Signal Name	XP85013 Name	Pin #	Signal Name	XP85013 Name	Pin #
VB	-	1	HVMON	-	2
SIB_DIN	-	3	SIB_CLK	-	4
P16	28	5	P32	48	6
P15	27	7	P31	47	8
P14	26	9	P30	46	10
P13	25	11	P29	45	12
P12	24	13	P28	44	14
P11	23	15	P27	43	16
P10	22	17	P26	42	18
P9	21	19	P25	41	20
P8	18	21	P24	38	22
P7	17	23	P23	37	24
P6	16	25	P22	36	26
P5	15	27	P21	35	28
P4	14	29	P20	34	30
P3	13	31	P19	33	32
P2	12	33	P18	32	34
P1	11	35	P17	31	36
SIB_DOUT	-	37	SIB_SYNC	-	38
SIBDAC	-	39	+5V	-	40

SIB Connector J2					
Signal Name	XP85013 Name	Pin #	Signal Name	XP85013 Name	Pin #
VB	-	1	HVMON	-	2
SIB_DIN	-	3	SIB_CLK	-	4
P48	68	5	P64	88	6
P47	67	7	P63	87	8
P46	66	9	P62	86	10
P45	65	11	P61	85	12
P44	64	13	P60	84	14
P43	63	15	P59	83	16
P42	62	17	P58	82	18
P41	61	19	P57	81	20
P40	58	21	P56	78	22
P39	57	23	P55	77	24
P38	56	25	P54	76	26
P37	55	27	P53	75	28
P36	54	29	P52	74	30
P35	53	31	P51	73	32
P34	52	33	P50	72	34
P33	51	35	P49	71	36
SIB_DOUT	-	37	SIB_SYNC	-	38
SIBDAC	-	39	+5V	-	40

Table 5: Sensor Interface Board (SIB) Connectors

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Mechanical Information

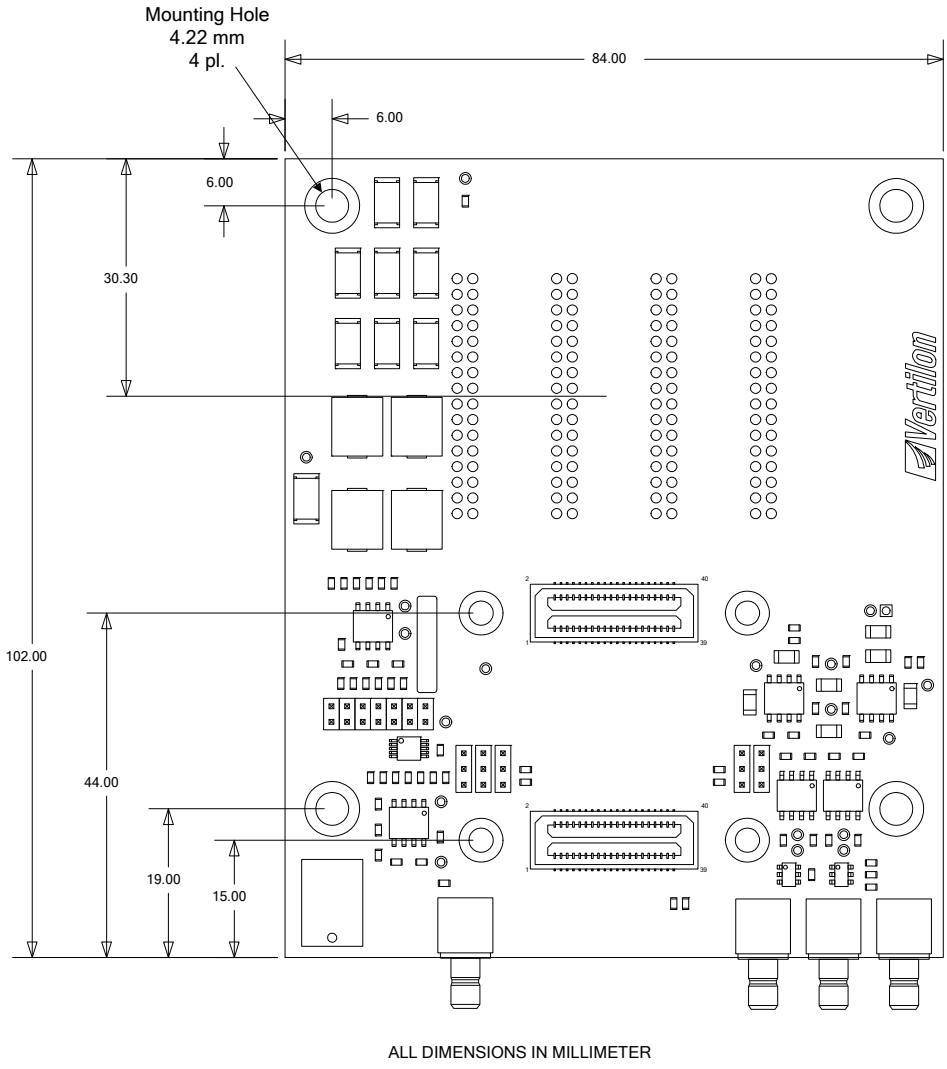

Figure 10: SIB264 Printed Circuit Board Dimensions

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