User Guide

SIB164A
64 Channel PMT Interface Board
Hamamatsu H7546B series

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Disclaimer

Vertilon Corporation has made every attempt to ensure that the information in this document is accurate and complete. Vertilon assumes no liability for errors or for any incidental, consequential, indirect, or special damages including, without limitation, loss of use, loss or alteration of data, delays, lost profits or savings, arising from the use of this document or the product which it accompanies.

Vertilon reserves the right to change this product without prior notice. No responsibility is assumed by Vertilon for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under the patent and proprietary information rights of Vertilon Corporation.

Copyright Information

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Table of Contents

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

List of Figures

List of Tables

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

General Safety Precautions

Use Proper Power Source

The SIB164A is powered with a +5V power source directly from Vertilon's PhotoniQ multi-channel data acquisition systems. Use with any other power source may result in damage to the product.

Operate Inputs within Specified Range

To avoid electric shock, fire hazard, or damage to the product, do not apply a voltage to any input outside of its specified range.

Electrostatic Discharge Sensitive

Electrostatic discharges may result in damage to the SIB164A. For these reasons, the SIB164A board is intended to be operated in a user's conductive instrument enclosure.

Do Not Operate in Wet or Damp Conditions

To avoid electric shock or damage to the product, do not operate in wet or damp conditions.

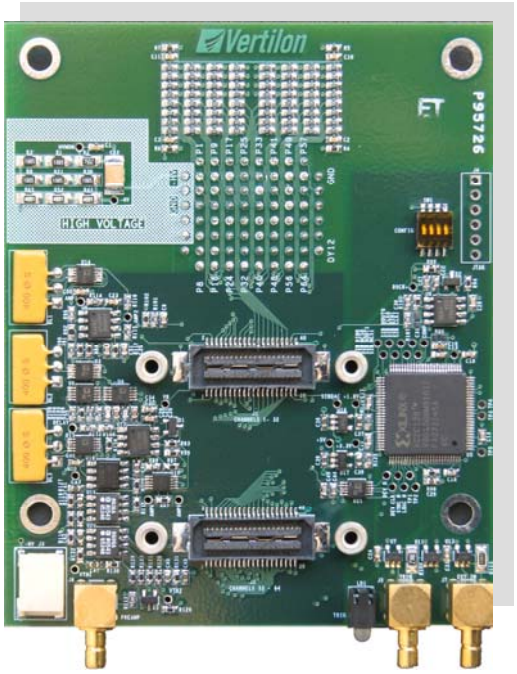
Do Not Operate in Explosive Atmosphere

To avoid injury or fire hazard, do not operate in an explosive atmosphere.

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Product Overview

- Interface board for Hamamatsu H7546B multianode PMT
- Provides 64 channel interface to data acquisition systems
- Separate high voltage input for PMT cathode bias
- High speed preamplifier for last dynode output
- Leading edge, constant fraction, and zero slope discriminators
- Adjustable discriminator gain and energy threshold
- 100% compatible with Vertilon's PhotoniQ multichannel DAQs
- No external power supply required
- Simplified control through PhotoniQ graphical user interface



The SIB164A multianode photomultiplier tube interface board provides the mechanical and electrical connectivity between the Hamamatsu H7546B 64 anode PMT and external signal processing electronics such as Vertilon's PhotoniQ multichannel data acquisition systems. The PMT is mounted to the bottom side of the SIB164A through 76 socket pins that connect the device's 64 anode signals, high voltage input, and last dynode output to the board. The anode signals are routed to two connectors located on the top of the board that each connect to a specialized high density coaxial cable assembly. This arrangement allows the SIB164A to be conveniently mounted directly into the user's optical setup with the PMT facing outward from the bottom of the board and the sensor interface board (SIB) cables exiting from the top. The SIB cables carry the 64 anodes from the PMT to the PhotoniQ where the charge from each is separately integrated, digitized, and sent to a PC for display or further signal processing. The negative high voltage bias to the PMT's cathode is supplied directly from the PhotoniQ on a high voltage cable to a dedicated connector on the SIB164A. For applications utilizing the last dynode output of the H7546B, the SIB164A includes a two stage high speed preamplifier whose output is available on an SMB connector. When specialized timing and triggering are required, this output can be connected to a separate external discriminator and triggering electronics. Alternatively, for more general purpose applications when the trigger requirements are not as stringent, one of the three on-board discriminators can be used. A leading edge, constant fraction, and zero slope discriminator — which respectively generate trigger signals based on a threshold, percentage of pulse height, and pulse peak — are available to the user. Several adjustments are included for optimizing preamp gain, discriminator gain, and discriminator energy thresholds. The full functionality and operation of the SIB164A is conveniently controlled through the PhotoniQ's graphical user interface. Intelligent software in the PhotoniQ constantly monitors the status of its SIB connectors to determine the type of sensor interface board attached to them. Once recognized, a dialog box specific to the recognized SIB is made available in the GUI through which the user has complete control over its operation.

The various functions on the SIB164A are described in greater detail on the following pages. When necessary, refer to the functional block diagram shown in Figure 1 below.

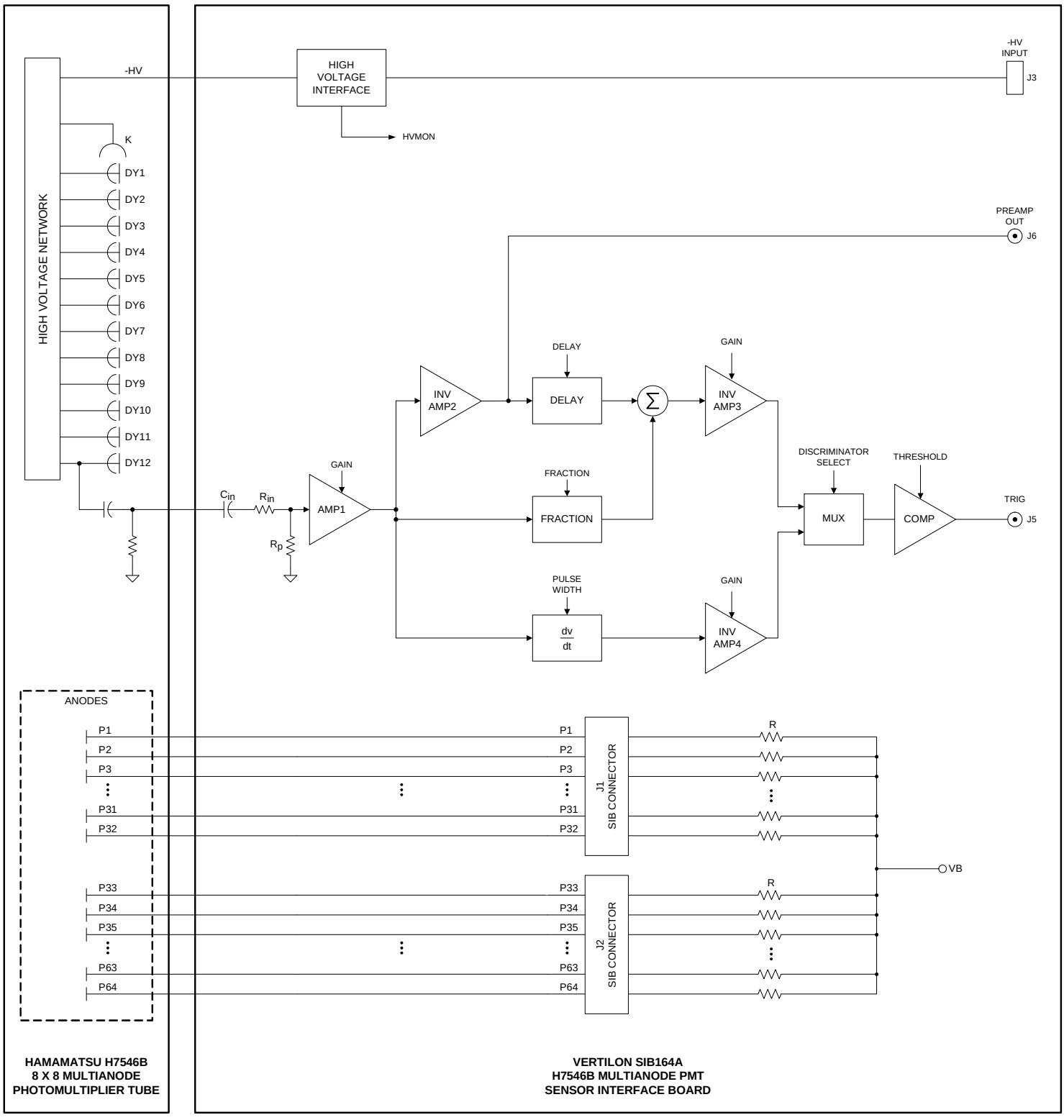


Figure 1: Functional Block Diagram

Specifications

(V_{supply} = +5.0V, T_A = +25C, unless otherwise noted)

Description	Sym	Min	Typ	Max	Units	Notes
HIGH VOLTAGE						
High Voltage Input Load Resistance			50		MΩ	Measured at high voltage input connector, J3.
HVMON to High Voltage Input Ratio			0.0015			±5%
ANODE CIRCUITS						
Quantity	P1 - P64		64			
Input Resistance	R		2.2		MΩ	
Input Bias Voltage	VB		+0.250		V	Detector bias voltage supplied from PhotoniQ data acquisition system.
LAST DYNODE PREAMPLIFIER						
Input Coupling Capacitance	C_{in}		0.1		uF	
Input Resistance	R_{in}		50		Ω	
Input Parallel Resistance	R_p		500		Ω	
Amplifier #1 Gain	A1	+3		+10	dB	
Amplifier #2 Inverting Gain	A2		0		dB	V_{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to last dynode preamplifier input (DY12).
Amplifier #2 Output Impedance			50		Ω	Measured at preamplifier output, J5
LEADING EDGE DISCRIMINATOR						
Threshold to Output Delay (V_{in}=100mV)	t_{d1}		10		nsec	
Jitter (V_{in}: 100mV)			500		psec	V_{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to last dynode preamplifier input (DY12).
CONSTANT FRACTION DISCRIMINATOR						
Delay Element	D		4		nsec	Standard delay element, other delays available.
Delay Range	D	0		12	nsec	
Delay to Fraction Ratio		0.12		0.50		
Amplifier #3 Inverting Gain	A3		+12		dB	
Threshold to Output Delay (V_{in}=100mV)	t_{d2}		35		nsec	
Time Walk (V_{in}: 30mV to 60mV)			-2.5		nsec	
Time Walk (V_{in}: 60mV to 150mV)			-1.5		nsec	V_{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to last dynode preamplifier input (DY12). Fraction set to 0.25, delay set to 3X, threshold set to 5%.
Jitter (V_{in}: 50mV)			500		psec	

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Description	Sym	Min	Typ	Max	Units	Notes
ZERO SLOPE DISCRIMINATOR						
Amplifier #4 Inverting Gain	A4		+20		dB	
Threshold to Output Delay (V_{in}=100mV)	t_{d3}		35		nsec	
Time Walk (V_{in}: 10mV to 80mV)			-5		nsec	V_{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to last dynode preamplifier input (DY12). Gain set to high, pulse width set to medium wide, threshold set to 10%.
Jitter (V_{in}: 80mV)			1		nsec	
TRIGGER OUTPUT						
Output Impedance			50		Ω	
Logic High Output Level	V_{OH}	+4.3	+4.8		V	(I_{OH} = -32mA)
Logic Low Output Level	V_{OL}		+0.2	+0.6	V	(I_{OL} = 32mA)
POWER						
Supply Voltage	V_{supply}	+4.9	+5.0	+5.1	V	
Supply Current	I_{supply}		75		mA	
DIMENSIONS						
Width	W		84		mm	
Length	L		102		mm	(not including SMB connectors which extend past PCB edge)
Thickness	T		1.57		mm	(printed circuit board only)

Table 1: Specifications

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Typical Setup

A typical setup using a SIB164A with a Hamamatsu H7546B PMT is shown below. The device is mounted to the SIB164A and positioned to detect incoming light from a scintillator crystal or optical assembly. Two SIB cables connect the 64 anode outputs from the SIB164A to a PhotoniQ IQSP482 or IQSP582 64 channel PMT data acquisition system. Through a USB 2.0 connection the digitized output data from the PhotoniQ is sent to a PC for display, logging, or real time processing. Additional connections between the SIB164A and PhotoniQ include a high voltage cable that provides up to 1000 volts of negative bias to the H7546B cathode, and a trigger cable that supplies the trigger to the PhotoniQ from one of the SIB164A's three discriminators. In an alternative configuration when precision timing or coincidence detection is required, an external discriminator with coincidence logic can be placed between the SIB164A preamplifier output and the PhotoniQ trigger input.

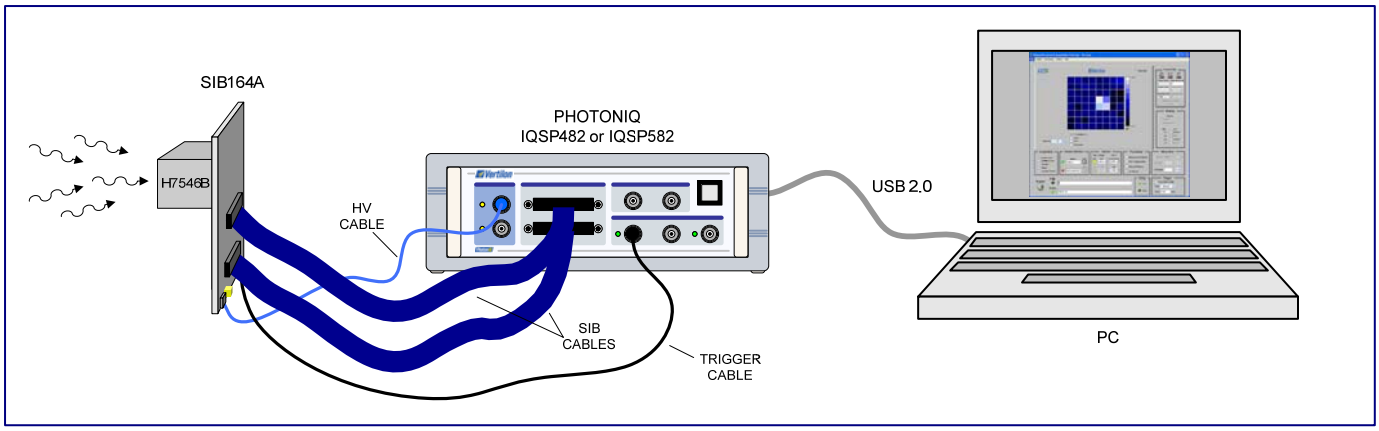


Figure 2: Typical Setup

High Voltage Interface

The SIB164A employs the interface circuit shown below between the high voltage input connector, J3, and the high voltage input to the H7546B. The monitor output (HVMON) allows the high voltage cathode bias for the PMT to be indirectly monitored at a reduced voltage level. Voltage readings at the monitor point should be scaled by a factor of 667. Calibration of the scale factor may be required.

Warning: The high voltage section of the SIB164A contains signals at voltage levels that can exceed negative 1000 volts. Never touch a component or signal in this area.

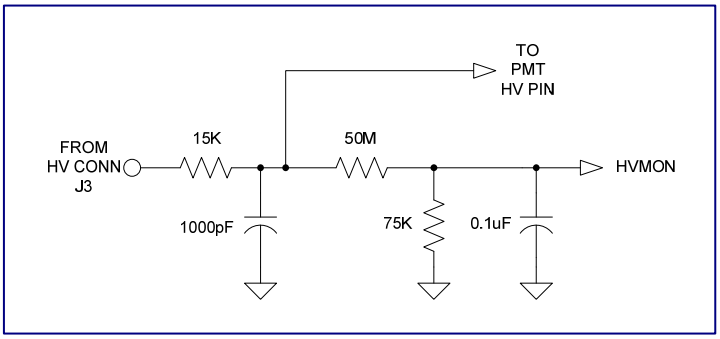


Figure 3: PMT High Voltage Interface Circuit

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Photomultiplier Tube Anode Circuits

The 64 anode signals (P1 – P64) from the PMT are routed directly on the SIB164A to two specialized connectors referred to as sensor interface board (SIB) connectors. Anodes P1 to P32 route to SIB connector J1 and anodes P33 to P64 route to SIB connector J2. Each SIB connector mates to a proprietary low-noise, high density SIB cable assembly that carries the 32 anode signals on coaxial connections to a Vertilon PhotoniQ 64 channel PMT data acquisition system. Depending on the required speed and dynamic range, either a PhotoniQ IQSP482 high dynamic range system or an IQSP582 high speed system can be used as the main data acquisition unit. To minimize the possibility of damage due to ESD, the PMT's anodes each have a 2.2 Mohm shunt resistor to a common low impedance point. This point is biased at a voltage equal to the bias voltage (VB) of the charge integrating transimpedance amplifiers on the PhotoniQ so that the PMT anodes can be DC coupled to them. Figure 4 below illustrates the equivalent circuit as seen by each PMT anode.

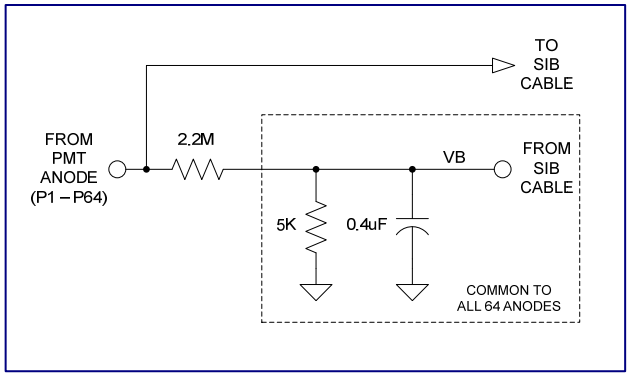


Figure 4: Anode Circuit

Last Dynode Preamplifier

This last dynode preamplifier is an inverting, AC-coupled, two-stage configuration whose input is designed for small positive voltage pulses from the last dynode (DY12) of the H7546B. The gain of the preamplifier is set by the user through the PhotoniQ GUI dialog box shown on the next page. For specialized applications requiring external discrimination or coincidence logic of the last dynode signal, the preamplifier output is available on SMB connector, J6. Alternatively, the preamplifier output can be further processed by one of the three different discriminators on the SIB164A to generate trigger signals in sync with the pulse on the last dynode.

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

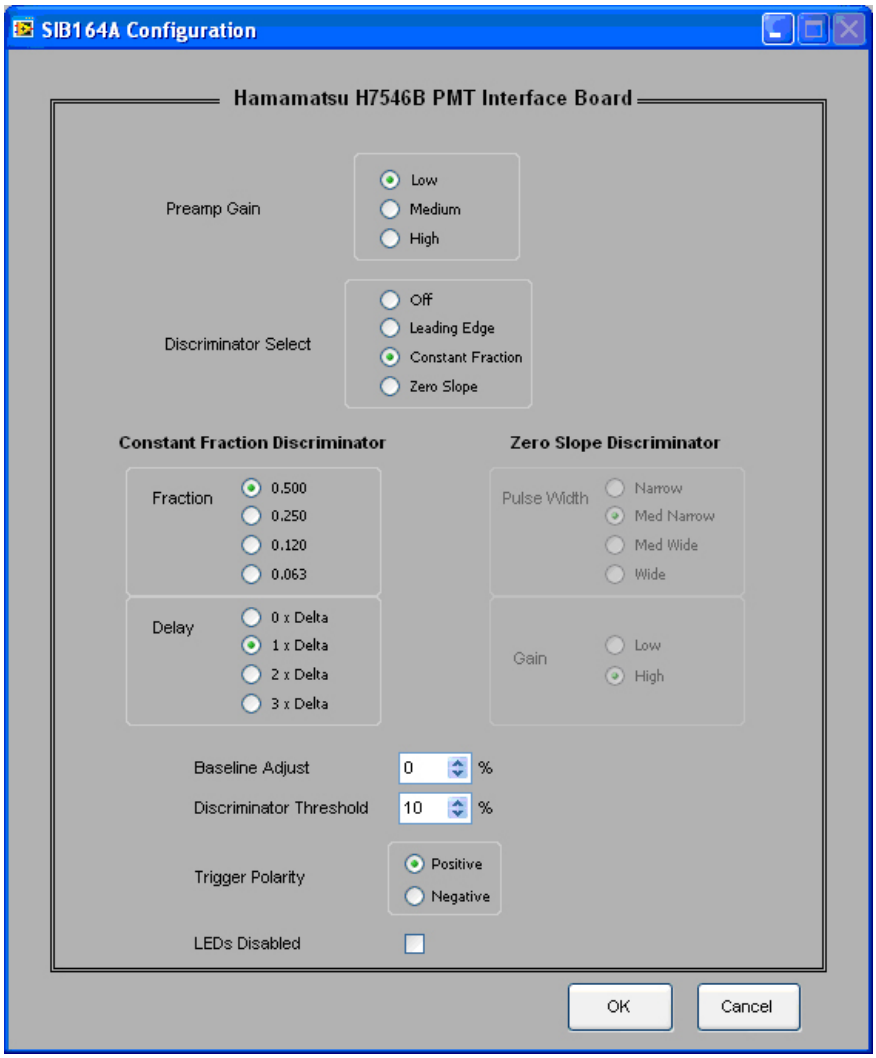


Figure 5: SIB164A Dialog Box

Leading Edge Discriminator

The leading edge discriminator is a simple timing circuit that generates a trigger signal when a charge pulse on the last dynode output from the H7546B PMT exceeds a user-defined threshold. It is implemented using a high speed comparator connected to the output of the last dynode preamplifier. Referring to Figure 6, negative going pulses from the preamplifier are compared to the discriminator threshold that is set through the SIB164A dialog box in the PhotoniQ GUI. A logic high (for *positive* polarity control) is generated on the trigger output (SMB connector J5) after a small delay (t_{d1}) from when the pulse first crosses the threshold, V_{th}. The trigger LED flashes indicating that a current pulse crossed the threshold. The discriminator switches back to a logic low when the pulse crosses the threshold from the opposite direction as it returns back to the baseline level. Because the trigger point is sensitive to the pulse height, this discriminator is typically used in applications that do not require precision timing.

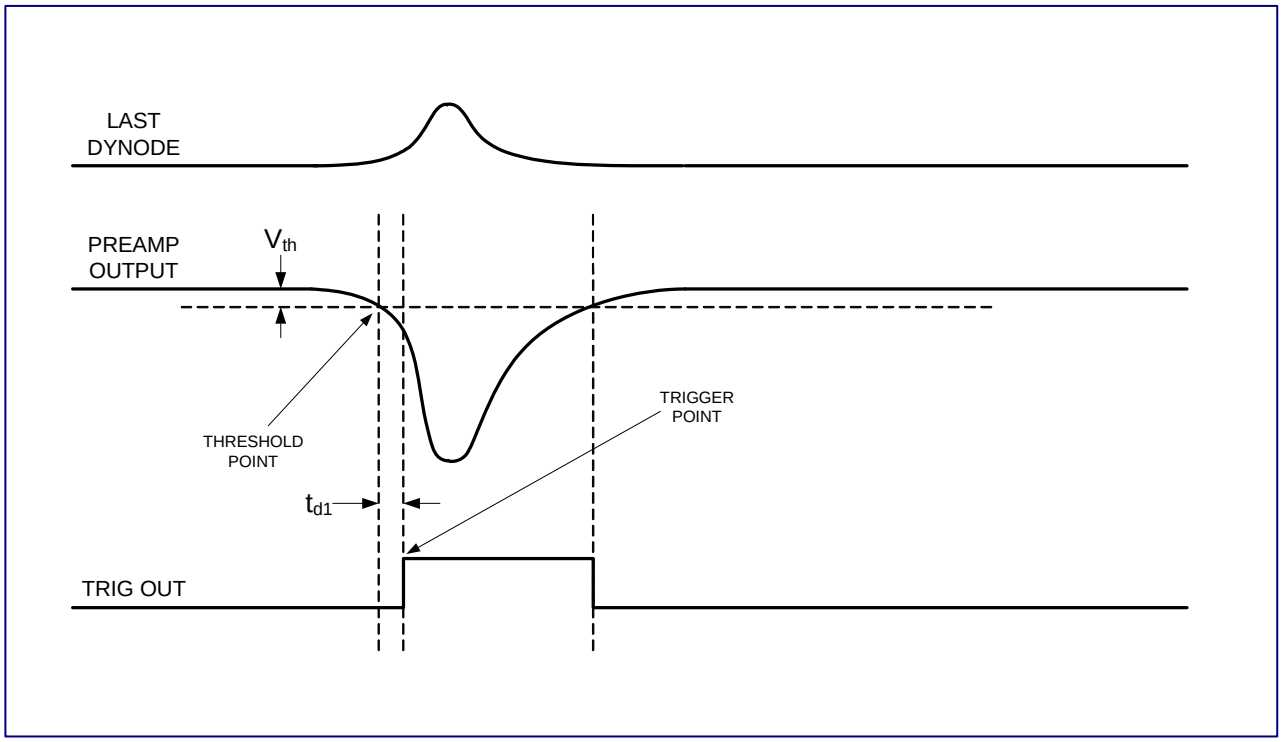


Figure 6: Leading Edge Discriminator Timing

Constant Fraction Discriminator

Unlike leading edge discriminators, a constant fraction discriminator (CFD) is capable of generating precisely timed trigger signals that are relatively independent of input pulse height. The CFD accomplishes this by subtracting a fraction of the input from a delayed version of the input such that the resulting signal always crosses zero at exactly the same point in time. The timing diagram in Figure 7 below illustrates the technique as implemented on the SIB164A. The CFD operates on the output of the last dynode preamplifier although technically only the delayed version of the signal (DELAY) is taken from the preamplifier output — the fractional part (FRACTION) is derived from the output of the first stage. The sum of these two components results in the AMP3 signal which is fed directly to the threshold comparator. This comparator compares AMP3 to a user-adjustable threshold voltage (V_{th}) which is used to arm the CFD and prepare it to generate the rising edge trigger signal when the AMP3 signal crosses the baseline level. By adjusting the delay time, fraction, and threshold (V_{th}) in the SIB164A dialog box, the CFD can be made to trigger at any reasonable percentage of the pulse height maximum.

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

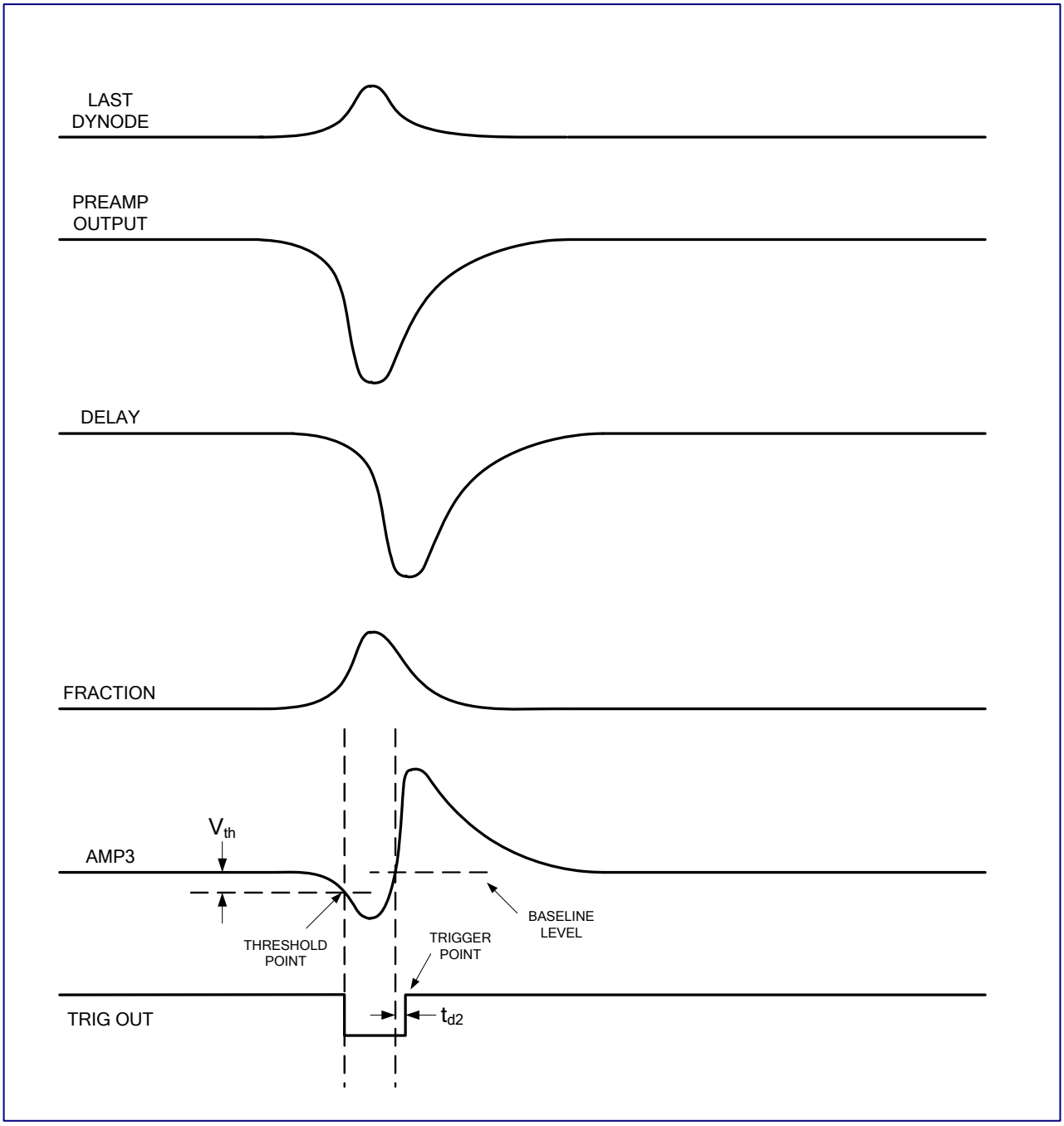


Figure 7: Constant Fraction Discriminator Timing

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Zero Slope Discriminator

The zero slope discriminator works by generating a trigger signal at the inflection point of the input pulse. It is this point where the pulse is at its peak and its slope transitions from positive to negative. Since AMP4 effectively operates on the derivative of the input pulse, its output crosses zero where the slope of the pulse is zero. This occurs at the pulse peak as shown in Figure 8. The threshold comparator compares AMP4 to the user-adjustable threshold (V_{th}) to arm the discriminator after which the trigger output fires when the AMP4 signal again crosses the baseline.

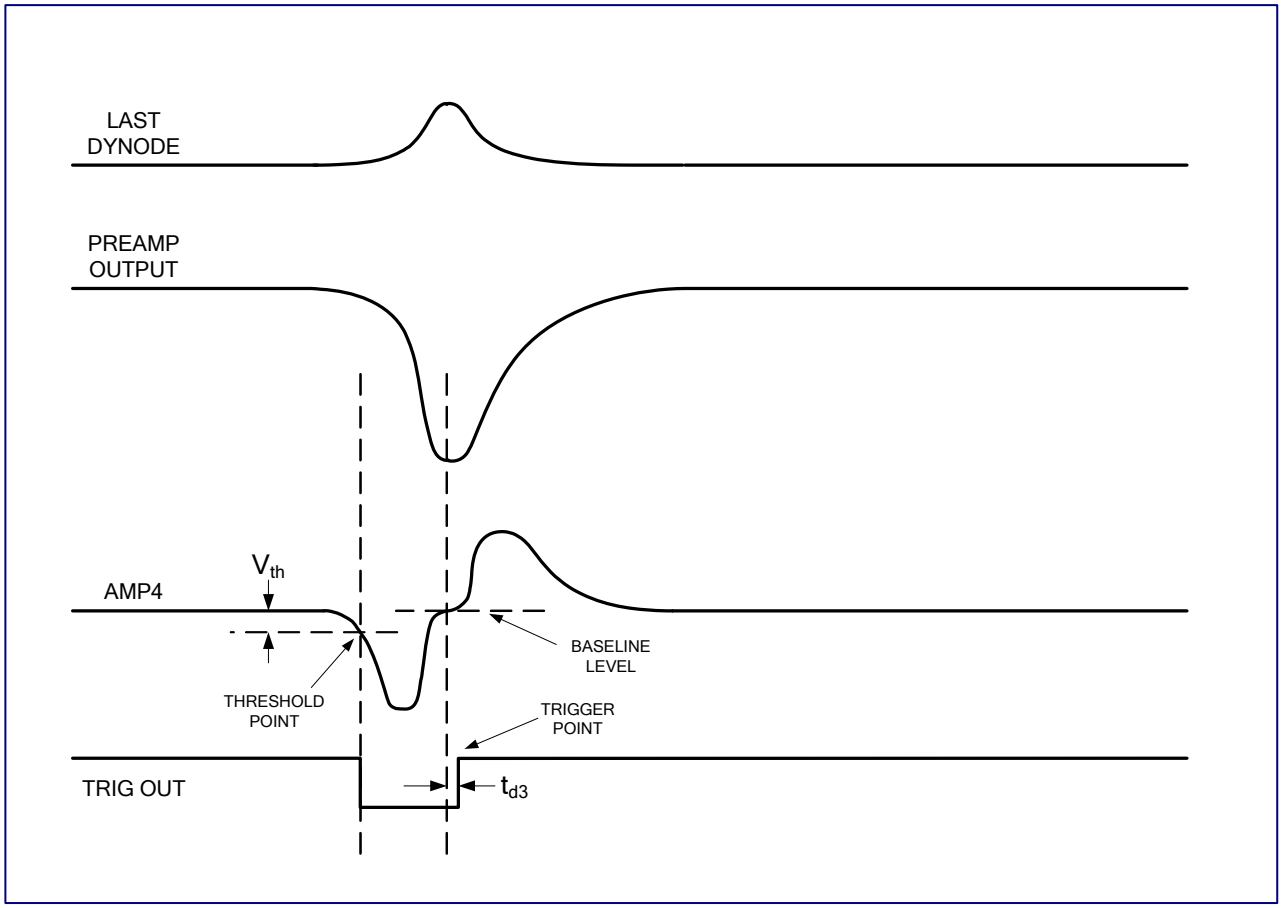


Figure 8: Zero Slope Discriminator Timing

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Top and Bottom Views

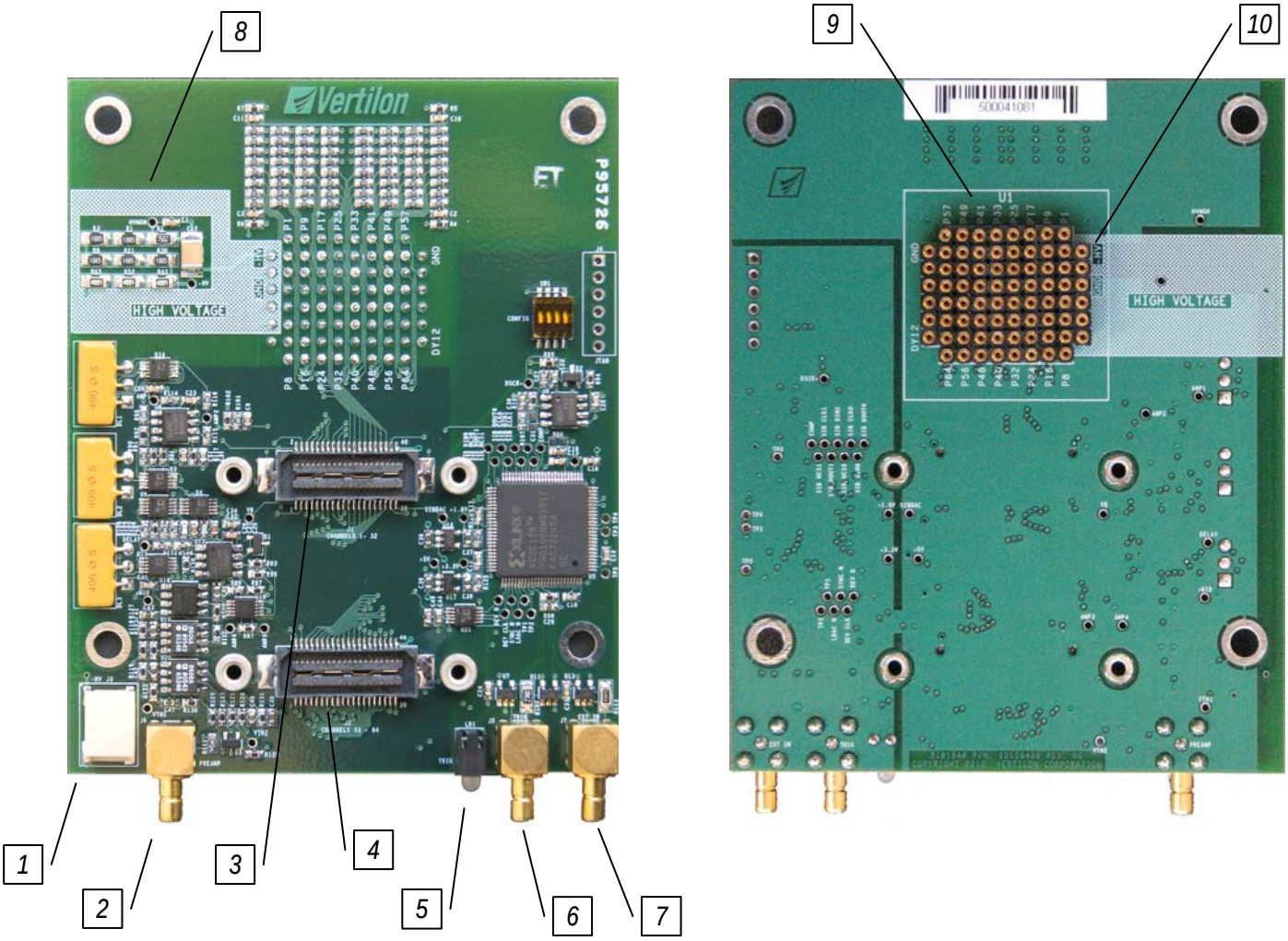


Figure 9: Top and Bottom Views

1. High Voltage Input (J3)
2. Preamp Output (J6)
3. Sensor Interface Board Connector (J1)
4. Sensor Interface Board Connector (J2)
5. Trigger Indicator LED
6. Trigger Output (J5)
7. External Input (J7)
8. High Voltage Section
9. H7546B Socket Connector
10. H7546B High Voltage Input

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Component Locations and Functions

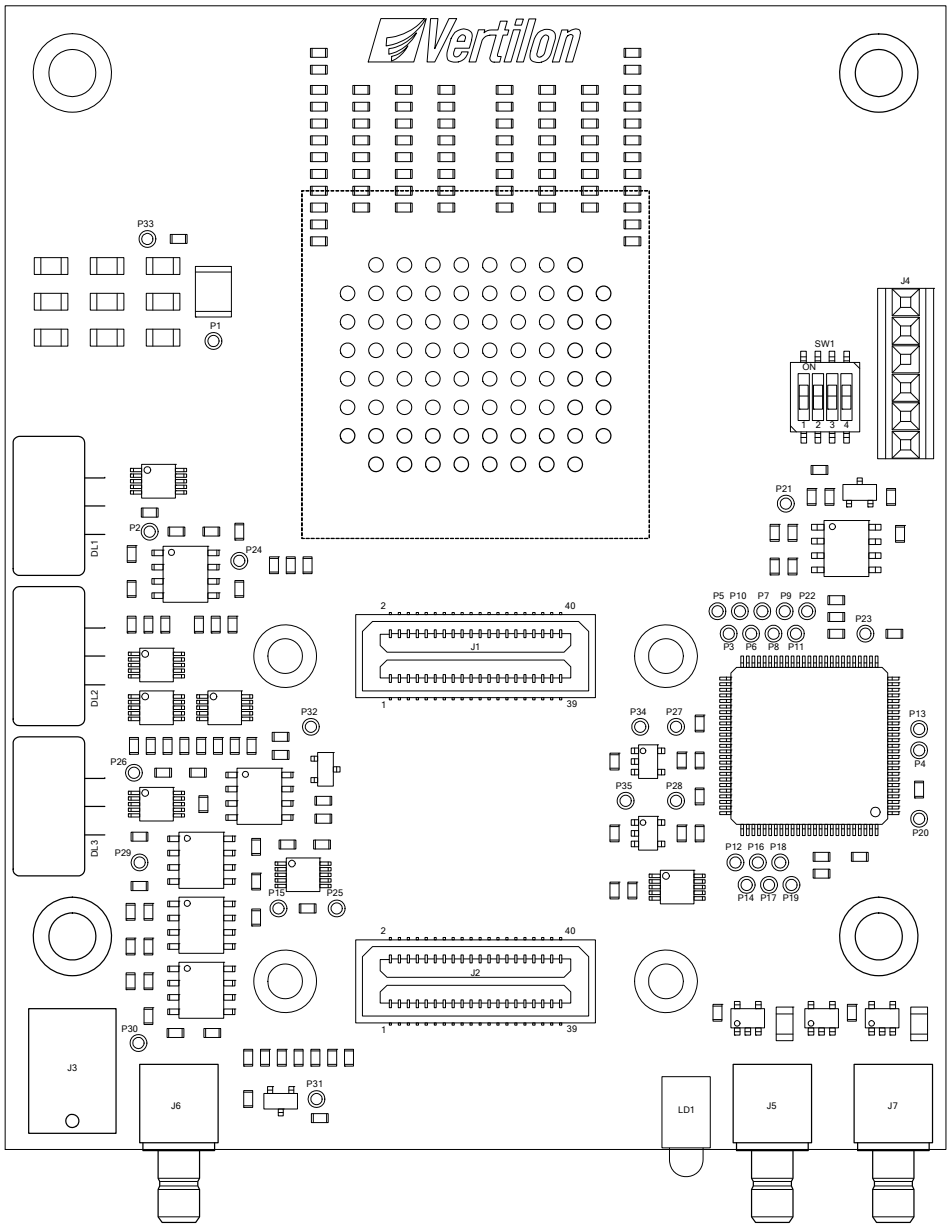


Figure 10: Component Locations and Functions

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Name	Function	Description
J1	CHANNELS 1 - 32	Sensor interface board connector to SIB cable for channels 1 -32
J2	CHANNELS 33 - 64	Sensor interface board connector to SIB cable for channels 33 - 64
J3	-HV	Negative high voltage bias input for PMT
J4	JTAG	JTAG interface
J5	TRIG	Trigger output
J6	PREAMP	Last dynode preamplifier output
J7	EXT IN	External Input (reserved for future use)

Table 2: Connectors

Name	Function	Description
LD1	TRIG OUT	LED indicator for trigger output
SW1: 1-2	DEV ADDR 1:0	Sets the device address for control by the PhotoniQ. Set both switches to “ON”.
SW1: 3-4	DEV TYPE 1:0	Sets the device type for control by the PhotoniQ. Set both switches to “ON”.

Table 3: Switches and LEDs

Name	Ref #	Description
+5V	P35	Main +5V power to the SIB164A supplied by the PhotoniQ through SIB connectors J1 and J2.
-HV	P1	PMT cathode bias. Warning: This is a high voltage point that can exceed negative 1400 volts.
HVMON	P33	Attenuated version of –HV used for indirectly monitoring PMT cathode bias.
VB	P32	Anode bias and reference voltage to the SIB164A supplied by the PhotoniQ through SIB connectors J1 and J2.
+MID	P29	Baseline voltage for last dynode signal processing chain. Nominally +2.0V.
VTH1	P30	Baseline level voltage (trimmed).
VTH2	P31	Discriminator threshold voltage.
AMP1	P2	Output of amplifier #1 in last dynode signal processing chain.
AMP2	P24	Output of amplifier #2 in last dynode signal processing chain.
AMP3	P25	Output of amplifier #3 in constant fraction discriminator.
AMP4	P15	Output of amplifier #4 in zero slope discriminator.
DELAY	P26	Output of constant fraction discriminator delay path. Reference to AMP2 to measure the delay.
COMP	P22	Discriminator comparator output.

Table 4: Test Points

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

SIB Connector Pinout

The SIB164A connectors and cables are fully compatible with all Vertilon PhotoniQ systems. For applications utilizing data acquisition systems other than Vertilon's PhotoniQ series, the pinout for connectors J1 and J2 is provided in Table 5 as a reference.

J1			
Signal Name	Pin #	Signal Name	Pin #
VB	1	HVMON	2
SIB_DIN0	3	SIB_CLK0	4
P16	5	P32	6
P15	7	P31	8
P14	9	P30	10
P13	11	P29	12
P12	13	P28	14
P11	15	P27	16
P10	17	P26	18
P9	19	P25	20
P8	21	P24	22
P7	23	P23	24
P6	25	P22	26
P5	27	P21	28
P4	29	P20	30
P3	31	P19	32
P2	33	P18	34
P1	35	P17	36
SIB_DOUT0	37	SIB_NCS0	38
SIBDAC	39	+5V	40

J2			
Signal Name	Pin #	Signal Name	Pin #
VB	1	HVMON	2
SIB_DIN1	3	SIB_CLK1	4
P48	5	P64	6
P47	7	P63	8
P46	9	P62	10
P45	11	P61	12
P44	13	P60	14
P43	15	P59	16
P42	17	P58	18
P41	19	P57	20
P40	21	P56	22
P39	23	P55	24
P38	25	P54	26
P37	27	P53	28
P36	29	P52	30
P35	31	P51	32
P34	33	P50	34
P33	35	P49	36
SIB_DOUT1	37	SIB_NCS1	38
SIBDAC	39	+5V	40

Table 5: Sensor Interface Board (SIB) Connectors

*Ground supplied through SIB cable shielding

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

Mechanical Information

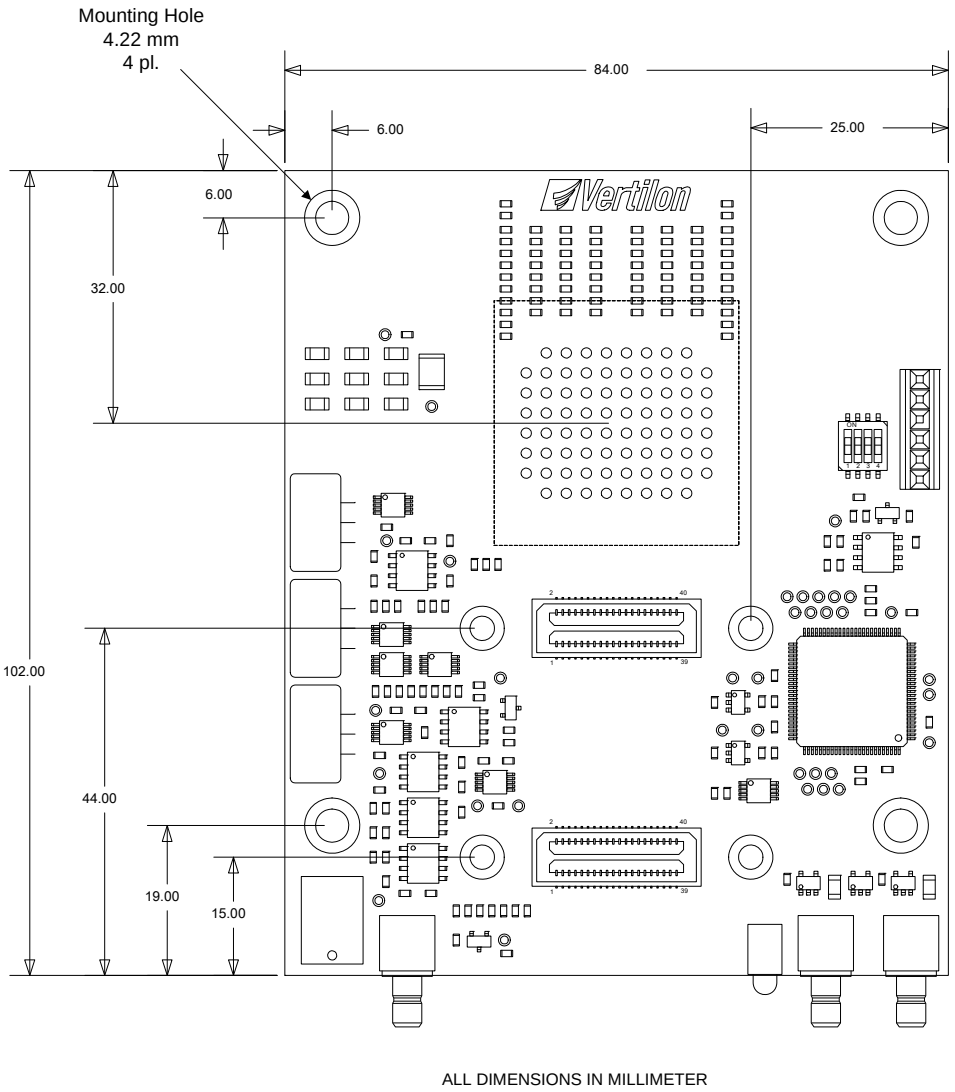


Figure 11: SIB164A Printed Circuit Board Dimensions

UG2849.1.3 Jan 2011

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com