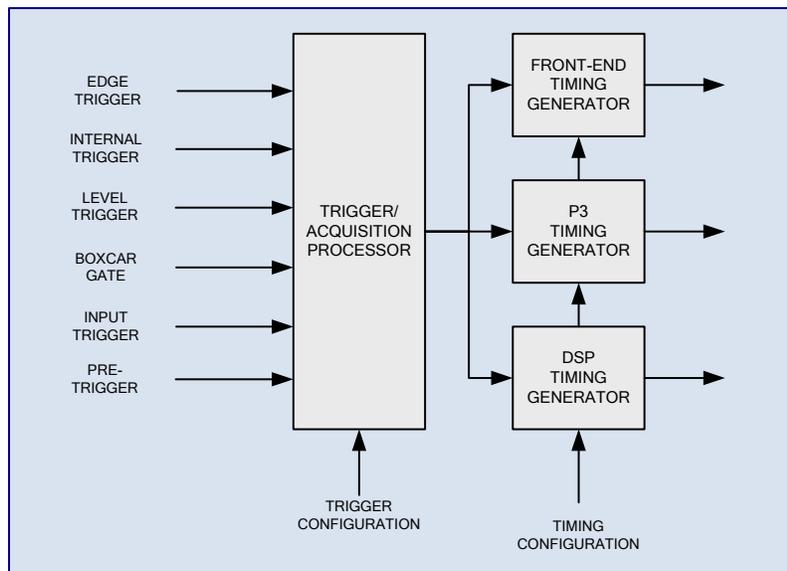


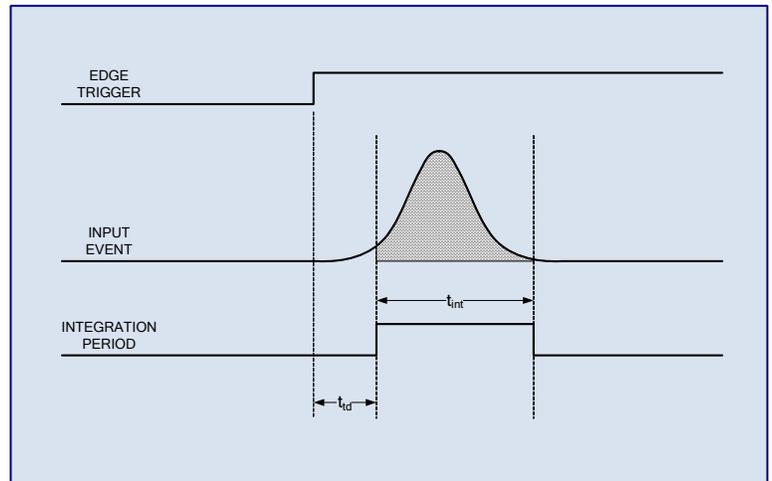
One of the most powerful features of the PhotoniQ is the wide variety of ways the data acquisition process can be triggered. The unit consists of an intelligent trigger module with the capability to trigger the input channels in conventional external or internal post trigger modes. Additionally, advanced on-board signal processing techniques permit more sophisticated triggering modes such as pre-trigger, which captures events that occur prior to the trigger signal, and input trigger, which captures events based on a threshold criteria for the event. The PhotoniQ also has a cross bank triggering mode that permits certain trigger parameters for each bank to be independently configured and operated. The descriptions below illustrate some of the advanced trigger and integration capabilities of the PhotoniQ.



Intelligent Trigger Module

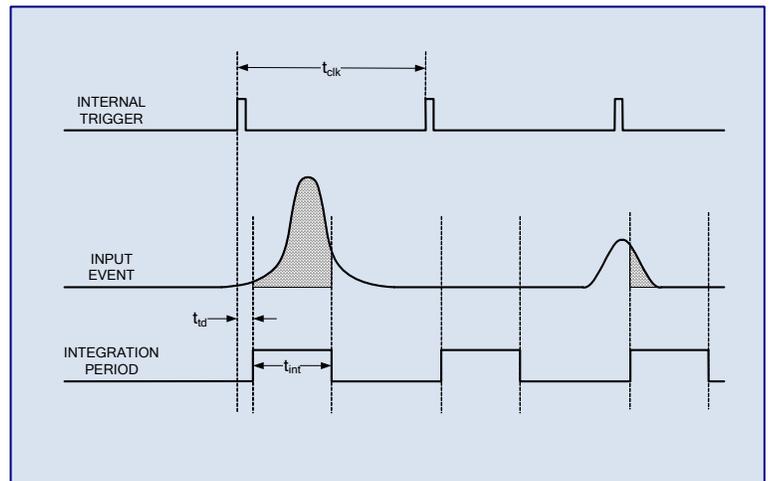
**Edge Trigger**

Edge trigger is a simple trigger mode whereby an externally-supplied positive signal edge to the intelligent trigger module starts the event acquisition process. As shown in the figure at right, the rising edge of the trigger initiates the start of the integration. The integration parameters of integration delay ( $t_{id}$ ) and integration period ( $t_{int}$ ) are programmable over a large range of values with very fine resolution.



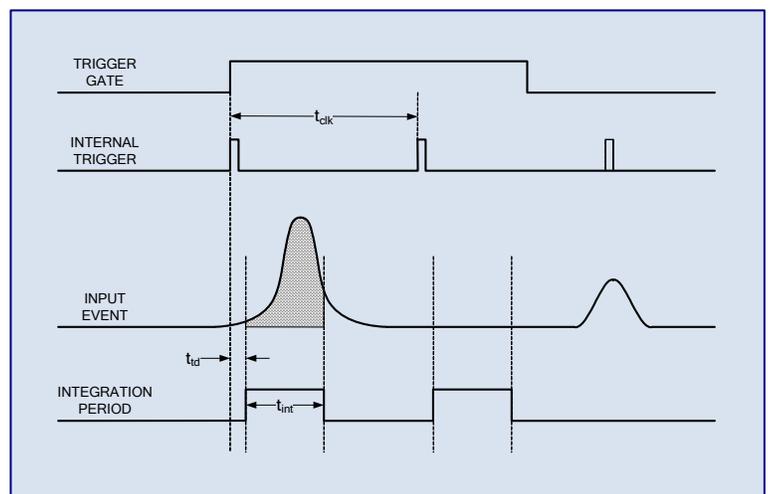
**Internal Trigger**

Continuous data acquisition is possible by operation of the unit in internal triggering mode. Here a programmable internal free running clock ( $t_{clk}$ ) replaces the external trigger signal. Data is continuously acquired on each edge of the clock signal. This mode is particularly useful when large blocks of event data are needed for collection and analysis, but no trigger signal is available.



**Level Trigger**

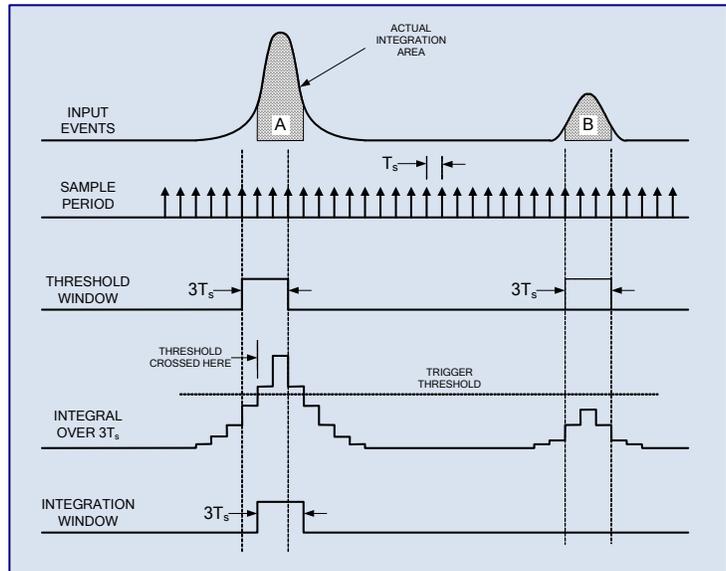
This trigger mode is similar to internal triggering except that an externally provided positive level-sensitive trigger gate controls the acquisition of events. The actual trigger signal is internally generated but synchronized and gated by the external trigger gate. A logic high enables the acquisition of events by allowing the internal trigger to generate the pre-programmed integration period. A logic low on the trigger gate blocks the internal trigger from generating the integration period so that no further events are acquired.



Input Trigger

Input trigger is used to trigger the acquisition process when incoming data on a specific channel exceeds a user defined threshold. No external trigger signal is required. The integration period determines the time over which the input signal is integrated and is typically set to closely match the expected pulse width. The figure shows a timing diagram for input triggering.

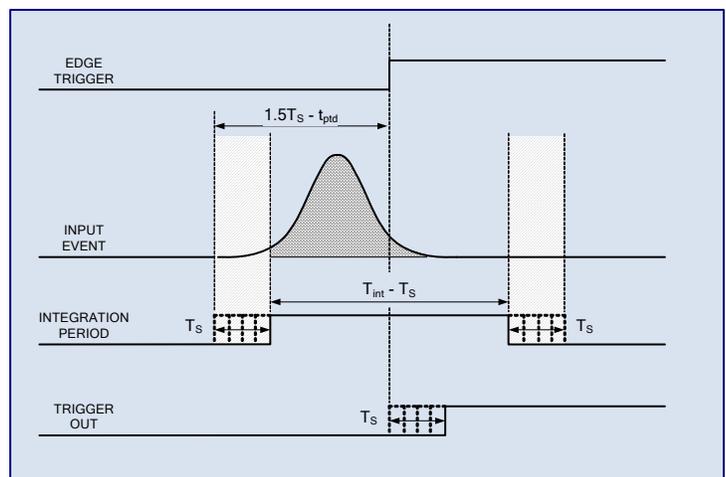
When using this mode, the integration period must always be a multiple of the sample period,  $T_s$ . The charge integrated during the integration time is compared to the trigger threshold level. In the example,  $t_{int}$  equals  $3T_s$  and event 'A' exceeds the threshold and event 'B' does not. The crossing of the threshold triggers the PhotoniQ to acquire data across all channels. To better position the integration window around the detected pulse, the actual window can be shifted by an integer number of  $T_s$  intervals (positive delay only) relative to when the threshold was crossed. In the example below, the integration window shift is one  $T_s$  interval.



Pre-Trigger

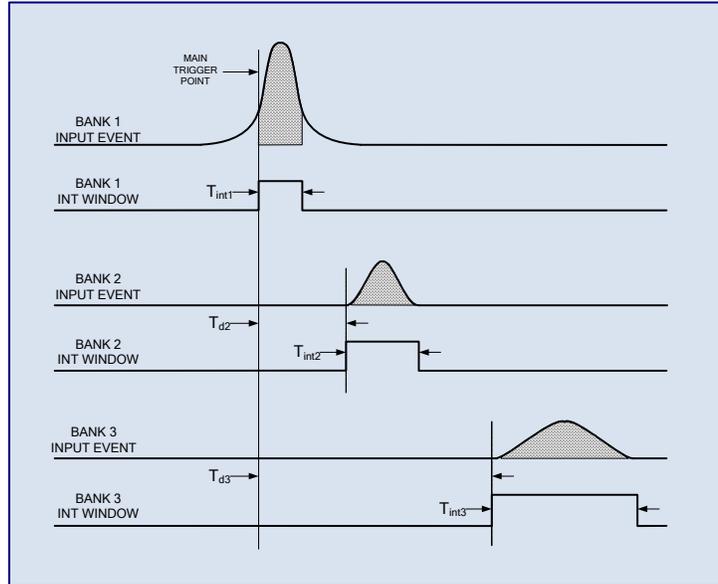
In pre-trigger mode, an external positive edge sensitive trigger signal is used to acquire event data that occurred prior to the trigger's arrival. As shown below, the programmable pre-trigger delay ( $t_{pid}$ ) is used to set the start of the programmable integration period ( $T_{int}$ ) at a time prior to the trigger edge. The pre-trigger uncertainty time ( $t_{ptu}$ ), shown as the dashed area in the figure, is equal to sampling period of the system,  $T_s$ . While the start of the integration period is uncertain by time  $T_s$ , the actual duration of the integration period itself is quite accurate. Both the pre-trigger delay and the integration period are constrained to be multiples of the system's sampling period. The trigger output signal is a reference signal that can be used to setup the system. Regardless of the pre-trigger delay time, the leading edge of the trigger out always occurs between 0 and  $T_s$  from the leading edge of the trigger input signal. The period of the trigger out is precisely equal to the integration time. When the pre-trigger delay is set to one (positive)  $T_s$ , the start of the integration period precedes the rising edge of the trigger output by one half of sample period,  $T_s$ . For other pre-trigger delay times (either positive or negative), the actual integration window is shifted accordingly.

Although pre-triggering mode is mostly used in applications where the integration window precedes the trigger edge (i.e. when the pre-trigger delay is negative), positive pre-trigger delays are also permissible. This positive delay mode has slightly lower noise than the edge trigger mode and can be used when precise control over the start (and end) of the integration period is not necessary.



**Cross Bank Triggering**

The flexibility of the PhotoniQ allows one or more channel banks to be triggered with one set of parameters which in turn trigger other banks using a different set of parameters. In a typical example, a bank is set up as an input trigger type with a particular integration period. The other banks are set up with different delays and integration periods. When an input event crosses the specified threshold on the first bank, the other banks can then be triggered. Data acquisition on these banks occurs with their respective specified delays and integration periods. The figure at right illustrates this example. Bank 1 is the main trigger bank and is setup as an input trigger type with an integration period of  $T_{int1}$  and integration delay of zero. Trigger timing for Bank 2 and Bank 3 is setup independently from Bank 1. The integration delay for these banks is  $T_{d2}$  and  $T_{d3}$ , respectively, and the integration period is  $T_{int2}$  and  $T_{int3}$ , respectively. For simplicity, Bank 4 is not shown. The main trigger point occurs when the signal on Bank 1 crosses the defined input threshold. From that point, Bank 2 and Bank 3 trigger after their defined integration delay time has elapsed. Each independently integrates over its defined integration period.

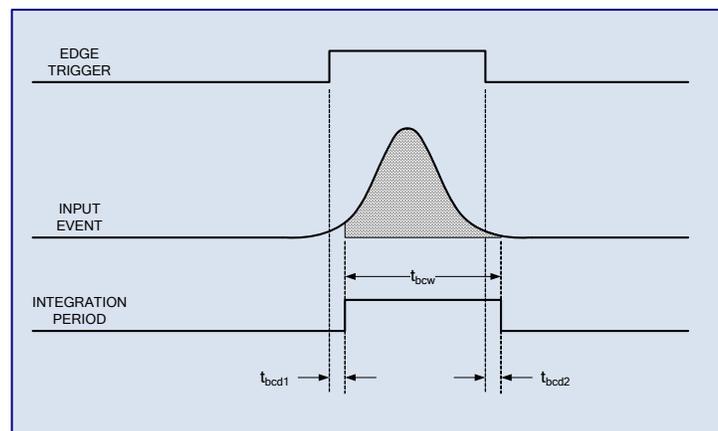


**Integration Delay and Period**

The integration delay is the parameter that sets the start of the integration period relative to the rising edge of the trigger. Only for pre-triggering can this value be negative. The integration period is the time duration over which the input signal is accumulated in the charge sensitive preamp. Both integration parameters are adjustable.

**Boxcar Mode**

Boxcar mode utilizes the input trigger signal to set the two integration parameters. The preset values are ignored. As shown in the figure, the trigger signal is used to define the period over which the input is to be integrated. Aside from a small amount of fixed positive delay (times  $t_{bcd1}$  and  $t_{bcd2}$ ), the boxcar formed by the trigger signal is the integration period ( $t_{bcw}$ ) and any unwanted background signals that occur when the boxcar is inactive are not integrated and effectively masked out.



**Boxcar Width**

The PhotoniQ has the ability to determine the width of the boxcar input signal. For each triggering event, the system measures the width of the boxcar and appends it to the event data in the log file if enabled. This feature is particularly useful for particle sizing where the boxcar is generated from threshold crossings on an external scatter channel. The sizing information (boxcar width) could then be used to normalize the spectral data.





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